Defect Detection Capability of Delay Tests for Path Delay Faults

Sreejit Chakravarty
Dept. of Computer Science
State University of New York
Buffalo, NY 14260
e-mail: sreejit@cs.buffalo.edu

Phone: 716 645 3180 ext 109
Fax: 716 645 3464.

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Abstract

Defects cause faulty static logic behaviour, faulty dynamic logic behaviour and elevated I_{DDQ} levels. Recent empirical and simulation studies show that adding at speed tests to test suites detects defective ICs missed by slow speed and I_{DDQ} tests. Delay tests for path delay faults and transition tests are two classes of tests that are often used for isolating ICs with faulty dynamic logic behaviour. We show that both these classes of tests often fail to detect many defects that causes faulty dynamic faulty behaviour. This implies that computing at speed tests is fundamentally different from computing delay tests for parametric testing and new techniques need to be developed.

1 Introduction

The objective of production testing is to detect manufacturing defects. Defects affect the static logic behaviour, dynamic logic behaviour, and also causes abnormal steady state supply current. Abnormal steady state supply current is detected by I_{DDQ} **Testing**[11, 13].

The input-output behaviour of circuits when driven at slow speed is referred to as **static logic behaviour**. A defect causing a change in the static logic behaviour of circuits is said to have caused faulty static logic behaviour. Faulty static logic behaviour is a manifestation of a change, due to a defect, in the logic function implemented by the circuit. Here, testing to detect faulty static logic behaviour is referred to as **logic testing** and the test sets used are referred to as **logic tests**.

The input-output behaviour of circuits when driven at close to its operating speed is its **dynamic logic behaviour**. A defect causing a change in the dynamic logic behaviour of circuits is said to have caused a change in the dynamic logic behaviour of circuits. Such faulty behaviour manifests itself when a transition, at an input, does not arrive at the primary outputs within a given interval of time. Here, testing to detect faulty dynamic logic behaviour, caused by defects, is referred to as **atspeed testing** and the test sets used are referred to as **atspeed tests**. We distinguish between atspeed testing and delay testing. In atspeed testing a defect is assumed to cause the circuit to malfunction. In delay testing the cumulative effect of parameter variations is assumed to cause the circuit to malfunction. Atspeed testing is sometimes referred to as ac-tests[17, 29].

To detect defective ICs, ICs should be subjected to a variety of tests. A reasonable test suite will inlcude logic testing, at-speed testing and I_{DDQ} testing[17, 29]. There is an ongoing study to ascertain the usefulness of including low voltage testing[2]. Recent empirical studies[17, 29] show that at-speed tests detect many defective ICs that are missed during logic and I_{DDQ} testing. Simulation studies also support this claim[2]. Here we ask ourselves the question: are the existing methods good enough to detect defects that causes faulty dynamic logic behaviour ? Similar questions can be asked for logic and I_{DDQ} tests. We do not address those issues here.

Currently, various techniques are used to compute at-speed tests. In some cases, the stuck-at test is run at high speed. Others apply functional vectors at high speed. A third approach computes pairs of stuck-at vectors, for selected lines in the circuit, and apply these pairs at-speed. They are referred to as transition tests[3]. Such tests were used in the experiments in [17].

Another possibility[17] is to use tests computed for delay testing. Such tests are computed using delay fault models[12, 19, 21] of which the most comprehensive is the path delay fault model. In the context of at-speed testing it is important to understand whether or not delay tests are good at detecting defects that causes faulty dynamic logic behaviour. **The main conclusion of this paper is that transition tests and delay tests often do not detect defects that causes faulty dynamic logic behaviour**.

The examples used will show that computing at-speed tests is a fundamentally different problem than computing delay tests. This prompts the question: what then is a good approach to computing at speed tests ? We do not attempt to answer this question here but concentrate on establishing the main point of the paper.

We need considerable back ground before we can present the main result of the paper. The required background is presented in sections 2 and 3. This is followed by a justification of our claim, respectively for opens and bridges, in sections 4, 5.

2 Characteristics of Delay Tests

Delay tests are computed using either the **path delay fault model**[25, 12, 27] or **gate delay fault model**[7, 31, 32, 8, 19, 9]. The path delay fault model is more comprehensive of the two and we assume this delay fault model in our discussion.

In the **path delay fault model**, along every physical path, from an input to an output of the combinational circuit, two distinct *transitions* - P_f, *input falling* and P_r, *input rising* - can propagate. For example, for the path $< e, n, q, s >$ of Figure 1(a) there are two path delay faults: $< e, n, q, s >_r$, input e rising and propagated along path $< e, n, q, s >$; and $< e, n, q, s >_f$, input e falling and propagated along path $< e, n, q, s >$. It was defined for parametric testing wherein we check if, for every physical path P, both P_f, P_r can propagate within a predetermined interval of time α.

Tests for delay faults consist of a pair of input vectors $< T1, T2 >$. As shown in Figure 2, first the **initialization vector** $T1$ is applied. All circuit signals are allowed to stabilize under its influence. Then the **test vector** $T2$ is applied. The circuit outputs are monitored for the appropriate transition in one of two ways: latch outputs after a time interval α, where α is the time-period of the operational clock; or use edge detection techniques to detect the presence of a transition during the period α.

Properties of delay tests are expressed using the set of notation Γ defined in Table 1. $T1(X), T2(X)$ are respectively the steady state values assigned to X by $T1, T2$. Note that

Logic Value	S0	S1	h0	h1	r	f	hr	hf
$T1(X)$	0	1	0	1	0	1	0	1
$T2(X)$	0	1	0	1	1	0	1	0
Hazard ?	No	No	Yes	Yes	No	No	Yes	Yes

Table 1: Definition of Γ, the set of logic values for delay testing

AND	$s0$	$s1$	$h0$	$h1$	r	f	hr	hf
$s0$	$s0$	$s0$	$s0$	$s0$	$s0$	$s0$	$s0$	$s0$
$s1$	$s0$	$s1$	$h0$	$h1$	r	f	hr	hf
$h0$	$s0$	$h0$	$h0$	$h0$	$h0$	$h0$	$h0$	$h0$
$h1$	$s0$	$h1$	$h0$	$h1$	hr	hf	hr	hf
r	$s0$	r	$h0$	hr	r	$h0$	hr	$h0$
f	$s0$	f	$h0$	hf	$h0$	f	$h0$	hf
hr	$s0$	hr	$h0$	hr	hr	$h0$	hr	$h0$
hf	$s0$	hf	$h0$	hf	$h0$	hf	$h0$	hf

Table 2: AND operation over Γ

r, hr (f, hf) distinguishes between a rising (falling) transition without hazard and with hazard respectively. Logic operations over Γ are easy to define. The AND operation is shown in Table 2.

In Figure 1(a), assume that the initialization vector $T1 = < a = 0, b = 0, c = 0, d = 1, e = 1, g = 1 >$ is applied prior to the vector $T2 = < a = 0, b = 0, c = 0, d = 1, e = 0, g = 1 >$. A falling transition at e propagates along the path $< e, n, q, s >$. The arrival time of the transition at s depends on the delay along $< e, n, q, s >$ and is independent of delays in the rest of the circuit[12]. This is an example of a **robust test**. Using the notation of Table 1, the logic value assigned by this test-pair to the lines in the circuit is shown in Figure 1(a). The test-pair is: $< a = S0, b = S0, c = S0, d = S1, e = f, g = S1 >$. On applying this input pair, if the falling edge at the output does not arrive before measurements are made then a delay fault exists along $< e, n, q, s >$. In Figure 1(b), the first falling edge at s can arrive only after the falling edge at q has arrived making the pair shown a robust test-pair for $< e, n, q, s >_f$.

Robust tests are classified as either **hazard-free** or **non-hazard-free**[20]. In Figure 1(a), lines g, d, c', m, p are inputs to gates that lie along $< e, n, q, s >$ but do not lie on

$< e, n, q, s >$. These are the **off-path inputs** of $< e, n, q, s >$. Under the arbitrary delay assumption if, on application of a robust test-pair T for path P no hazard occurs at the off-path inputs of P, as in Figure 1(a), then T is a **hazard-free robust test-pair** for P.

Both hazard-free and non-hazard-free test-pairs can be used to detect delay faults. However, we have to be careful in using them. If the output of the circuit is sampled after time α, following the application of $T2$, then only hazard-free robust test-pairs can be used. This is because, in Figure 1(b), the hazard could result in the sampling of an incorrect value. On the other hand, if edge detection is used to signify the arrival of a transition during the α interval, following the application of $T2$, then hazards can be allowed at the output. In this case, both types of test-pairs can be used.

There are two kinds of hazard-free robust test-pairs[20, 21]. In Figure 1(a) the falling transition at e propagates along only one path $< e, n, q, s >$. This is an example of a **single path propagating hazard-free robust test-pair**. In Figure 1(c) the falling transition at e propagates along multiple paths $< e, n, q, s >$ and $< e, k, p, s >$. The falling edge at s can arrive only after both the falling edges at p, q has arrived. Thus, it is an example of a **multiple path propagating hazard-free robust test-pair** for both $< e, n, q, s >_f$ and $< e, k, p, s >_f$. We next look at properties that must be satisfied by the two types of hazard-free robust test-pairs.

- An input pair $T =< T1, T2 >$ is a **multiple path propagating hazard-free robust test** for input rising (falling) delay fault along path p if and only if: T causes a rising (falling) transition at the input of p; and T satisfies the constraints of Figure 3(a)[20]. In Figure 3(a) the gate is assumed to be on the path p and A(B) is the on-path (off-path) input of this gate. For example, if the gate is an AND gate, and there is a rising transition at A then each off-path input, that is also an input of this gate, must have either a rising transition or hazard free $S1$.

- An input pair $T =< T1, T2 >$ is a **single path propagating hazard-free robust test-pair** for input rising (falling) delay fault along path p if and only if: T results in a rising (falling) transition at the input of p; and T satisfies the constraints of Figure 3(b)[20]. Thus, if the gate is an AND gate and A has a rising transition then each off-path input that is also an input to this gate must have a hazard free $S1$.

	a	b	c	d
1	S0	S1	r	S1
2	S0	S1	r	f
3	S0	S1	r	r
4	S0	r	r	S1
5	f	r	r	S1

Table 3: Quality of delay tests

The above constraints on the test-pairs is henceforth referred to as **hazard-free robust propagation constriant**. In addition to this, robust test-pairs have to satisfy some additional constraints[18]. For the path delay fault $< c, e, g >_r$ of Figure 5(a) there are a number of hazard-free robust test-pairs. Some of them are listed in Table 3. The question is: other than the fact that some of them are hazard-free robust test-pairs for a number of other paths, is there a difference in the capability of these tests to detect the path delay fault $< c, e, g >_r$? We say that test-pair a is better than test-pair b, for the path delay fault $< c, e, g >_r$, if and only if a wider range of delays along this path is detected by a when compared with b.

To understand why one of these test-pairs will be better than another we need to define **off-path input**, **side fanout gate** and **side fanout node**. Figure 5(b) defines them, assuming that the path under test is shown using bold lines. The first important conclusion, based on simulation results[18], is that: **the propagation delay along a path depends on the values at the side-fanout-node**. The first three test-pairs of Table 3 are single path propagating hazard-free robust test-pairs for the path delay fault $< c, e, g >_r$. They however differ in the values they assign to the side-fanout-node d and will differ in the range of delay defects they can detect.

The second important conclusion is that the delay along a path **depends on the values assigned to the off-path inputs**. The 4th, 5th test-pairs of Table 3 are test-pairs that differ in the values they assign to the off-path inputs a, b. These two tests will therefore detect different ranges of delay variations for the path delay fault $< c, e, g >_r$.

A third important conclusion is that the vector prior to applying the test-pair (**pre-initializing test**) is also important in ascertaining the effectiveness of the test-pair. This is based on the following observation[18]. The switch-level circuit for gate E is shown in Figure 5(c). Node q is an **internal node**. The propagation delay of a transition from b to

e is affected by the voltage at the internal node q. Node q could be at 0 (b=1), floating (b=c=0) or a weak 1 because of charge charing between e, q (c=1,b=0). If $b = c = 0$ and q is floating then the voltage at q is a function of the pre-initializing test. To determine whether test-pair 1 or 4 of Table 3 is better we have to know what the pre-initializing test was.

Thus, to detect the smallest variation along path p test-pairs, in addition to satisfying the hazard-free robust propagation constraints, has to satisfy some additional constraints. These constraints on the values assigned to the off-path inputs, side fanout nodes, and pre-initializing test are henceforth referred to as **quality constraints**.

Subsequently, we assume that: delay tests are computed using the path delay fault model; they are robust and hazard-free; they can be either single path propagating or multiple path propagating; and satisfy both the quality and the hazard-free propagation constraints.

For a line x in the circuit there are two kind of ac-tests - one for a rising transition at x, and another for a falling transition at x. Let T_0 (T_1) be a test for x s-a-0 (x s-a-1). Then the two ac-test pairs are: $< T_0, T_1 >, < T_1, T_0 >$.

3 Defects

The dominant failure modes in VLSI circuits are opens and shorts[14, 15]. In the next two subsections we summarize what is known about the behaviour of VLSI circuits in the presence of shorts and opens. In addition to these defects other defects which are less frequent are[28]: punch throughs, parasitic transistor leaks, defective pn junctions, incorrect threshold voltages etc.

3.1 Shorts

Shorts, also referred to as bridges, occur when two or more distinct nodes of the circuit get connected due to a defect. Shorts occur when dust or extra material is deposited during fabrication. It also occurs due to imperfections in the mask, imperfections in the etching process etc. These defects connect two distinct nets on the same layer. Nodes having patterns on two adjacent layers can also get shorted. This happens when the insulating layer between adjacent layers break down or is not formed properly.

If a node of a gate is slow-to-rise (slow-to-fall) then we have a **slow-to-rise** (**slow-to-**

fall) transition fault. Simulation studies, using the behaviour of the two input NAND gate of Figure 6(a), for the short between its two inputs X, Y are presented in [30]. If $UV = 01$ and pulldown strength of N2 is larger than the pullup strength of P1 (n-dominant) then the static behaviour is not affected. On the other hand if the pulldown strength of N2 is smaller than the pullup strength of P1 (p-dominant), for some values of the short resistance and some input vectors, the defective circuit exhibits Y s-a-1 behaviour. Assume that the input combination $UV = 11$ is applied followed by $UV = 01$. This attempts to create a rising transition at X. However, because of the presence of the short there is a conducting path from X to Gnd. This creates a slow-to-rise transition fault at X. The presence of this short can also lead to a slow-to-fall transition fault at Y. This transition fault is activated if the input vector $UV = 00$ is applied followed by the input vector $UV = 01$. The presence of the activated path from Y to V_{DD} through the short delays the fall of Y. If X or Y fans out this defect manifests itself as a **multiple transition fault**. It also maps onto different transition faults depending on the way the defects are activated.

The above examples considered shorts between two gate outputs (**external shorts**). Intra-gate shorts that we discuss involve shorts between the three terminals of an individual transistor. Thus we have gate-source(GS), gate-drain(GD) and source-drain(SD) shorts per transistor. Shorts labeled $b1, b2$ and $b3$ of Figure 6(b) are examples respectively of GS, GD and SD shorts. This example is a modification of an example from [4]. Note that GS, GD are different from gate-oxide shorts. When we consider GS or GD, unlike a gate-oxide short, we assume that the transistor is fully functional and equivalent to the fault-free transistor. We discuss the effect defect $b1$ has on the circuit performance.

Defect $b1$ affects the static and dynamic logic behaviour of the circuit. Assume that the short resistance is very small. Then V_{AC} is very small (below the cut-off voltage for FT) and FT does not conduct. The output Y of the gate cannot discharge and FT is said to be **stuck-open**. So tests for stuck-open faults can detect such defects. If the pullup strength of gate A is small and the pulldown strength of transistor $T1$ is large then the defect manifests itself as A stuck-at 0 for some input vectors.

If the pullup strength of gate A is comparable to the pulldown strength of $T1$ then node A has a degraded voltage much below V_{DD} (**intermediate**). This can delay a transition from propagating from D to W because of the following reason. Both the transistors in gate W driven by A is turned on very weakly. Assume that the input vector $DUV = 000$ is applied followed by the input vector $DUV = 100$. This rising transition at D will result in a slow-to-fall transition at W because of the weakly conducting transistor in gate W driven by A. This example is interesting because it shows that the effect of the defect can "spill over" into a gate in which the defect is not located.

As the short resistance increases, V_{AC} can vary over a larger range. Therefore, instead of being cut-off FT conducts weakly. This leads to a slow-to-fall transition fault at Y when UV is changed from 10 to 00. Since A remains at an intermediate level, as explained above, a slow-to-fall transition fault could also appear at W.

In summary, depending on its resistance and location, a short can cause: faulty static logic behaviour, multiple transition fault, transition faults in gates where the short is not located etc.

3.2 Opens

Open circuit defects, or opens as we refer to them here, are unintentional discontinuities. Such defects splits a node into two or more distinct nodes. They are caused by missing metal, poly or diffusion which occurs due to improper etching, masking error, electro-migration etc. There are two types of opens - **narrow** and **large**. When the opening is large no current can flow between the two ends of the open when a voltage is applied across it[6, 16]. For narrow openings (< 100 nm) a small leakage current, due to tunneling effect, flows across the open[6].

The impact of open defects on the performance of the circuit is a function of the location and size of the defect, as well as the the electrical parameters of the circuits. In our discussion we use the opens marked $d1 \ldots d6$ in Figure 7. Defects at $d2, d3$ are respectively **open-gate** defects in transistors $P1, N1$. We refer to $d4(d6)$ as **open-pnet** (**open-nnet**) defect. Defect $d5$ is an **open-output** defect. Defect $d1$ is an **open-source** defect for $N1$. It is also an **open-drain** defect for $N2$. Each of these defects have a different impact on the performance of the circuit which we discuss next.

Open-source: Assume $d1$ of Figure 7 is a narrow open and we apply the sequence of input vectors that sets GF to 00 followed by 11. H is charged to 1 followed by a slow decay of V_H, the voltage at H. Therefore $d1$ can manifest itself as a slow-to-fall transition fault.

Open-drain: Open-drains are very similar to open-sources and the above discussion about open-source applies.

Open-pnet: Consider $d4$ of Figure 7 and assume it is a narrow open. The defect manifests itself as a slow-to-rise transition fault. This malfunction can be activated by setting GF to 11 followed by setting GF to 10.

Open-gate: Open-gate defects result in a transistor whose gate is not driven by either a primary input or the output of a gate. Such transistors are known as **floating-gate transistors**. The behaviour of transistors with floating gates have been studied extensively [1, 22, 24, 10, 6]. A study concluded that floating gates acquired voltages below the cut-off of the n-transistor[6]. This implies that floating gate transistors do not conduct. Subsequently, measured gate voltages in the range 0.38 to 2.3V have been reported[10]. This suggests that a floating gate transistor could either be conducting or not conducting at all. Experimental results in [26] concludes that the floating gate transistor is cut-off.

The above results, at a first glance, appears very confusing. These results can be explained by the fact that the voltage at a floating gate is a complex function of the "environment" it is in. Detailed analysis of the effect of the "environment" on the floating gate voltage can be found in [22, 1, 24]. The final conclusion is that an FET with a floating gate could be in one of three states: non-conducting, conducting weakly and conducting strongly.

Defect $d3$ of Figure 7 is an example of a defect such that $N1$ becomes a floating gate transistor. If such FETs conduct strongly or weakly it can can lead to a degraded voltage level at H, for some input vectors. The degraded voltage levels, as we have seen in the case of shorts, can result in a change in the static or dynamic logic behaviour.

Open-output: Exemplified by defect $d5$ in Figure 7 such defects result in complementary pair of transistors, like $P1, N1$, to float. Since the defect lengths are generally large and the overlap with metal is also high such transistor pairs conduct strongly. Thus, as seen in the case of shorts and other opens, they can affect the static and dynamic logic behaviour of circuits.

4 Delay Tests and Opens

We investigate the detection capability of delay tests to detect opens. We will see, through a series of examples, that in order to detect opens delay tests have to satisfy additional constraints. These constraints are such that they are not necessarily satisfied by hazard-free robust test pairs. In addition, there are defects for which the test pairs have to violate the hazard-free conditions. Two kind of opens are considered - open gates and open outputs.

4.1 Open Gate

For these examples assume that the opens are large opens. First consider defect $d1$ of Figure 8(a) where the gate of $N1$ is open. Then, $N1$ can either not conduct, conduct weakly or conduct strongly. Assume that the defect is such that it causes N1 to conduct strongly.

Depending on the characteristics of $P1, N1, N2$, an input vector that sets h, k to 1, 0 respectively results in a weak 1 at p. Thus, the static logic behaviour of the circuit is not affected. However, the dynamic logic behaviour is affected. The weak 1 at p causes the transitor pair $N3, P3$, in gate S driven by p, to conduct weakly. This delays a falling transition, due to a rising transition at q, from propagating to s.

In order to activate the defect the second vector of the test-pair should set p to 1 by setting h, k to $1, 0$ respectively. Thus, hazard-free robust test-pair for a path delay fault, along a path passing through q, and causing a rising transition at q, detects the defect during delay testing provided it also satisfies an additional constraint. That constraint is that the second vector sets h, k to 1,0 respectively. It can be verified using Figure 8(b) that $< a = S0, b = f, c = S0, d = S0 >$ is one such test-pair. On the other hand the test-pair $< a = S1, b = f, c = S0, d = S0 >$, which is a hazard-free robust test-pair for a path delay fault traversing q that causes a rising transition at q, does not detect defect $d1$.

The additional constraint needed to "activate" the defect is interesting for the following reason. The constraints are on lines h, k which are neither off-path nor side fanout nodes of the path $< e, n, q, s >$. Therefore, the constraint does not qualify either as a hazard-free propagation or quality constraint. **Hence, even if we compute delay tests that satisfy both the constraints it is not guaranteed to detect this defect.**

It is easy to see that **no ac-test or transition test for q rising detects this defect since no stuck-at test for a is guaranteed to set h, k to $1, 0$ respectively.**

Next let us consider defect $d2$ of Figure 8(a) where the gate of $P1$ is open. Once again, $P1$ can either not conduct, conduct weakly or conduct strongly. Assume that the defect is such that it causes $P1$ to conduct weakly. In this case depending on the characteristics of $P1, N1, N2$, any input vector that sets both h, k to 1 results in an intermediate voltage at p. Thus, for some characteristics of $P1, N1, N2$, it may be d etectable as a p stuck-at 1 fault during logic testing. For a wide range of intermediate voltages at P it will affect the dynamic behaviour and not the static behaviour. The intermediate voltage at p causes the transistor pairs $P3, N3$, in gate S driven by p, to conduct weakly. This, in turn, delays a falling transition, due to a rising transition at q, to propagate to s. In order to activate the defect the second vector of the test-pair should set both h, k to 1, in the fault free case. Thus, analogous to defect $d1$, a hazard-free robust test-pair for the path delay fault that causes a rising transition at q detects the defect during delay testing. However, the additional constraint that it must satisfy is different in that the second vector should set both h, k to 1.

Once again note that the constraints are on lines h, k which are neither off-path nor side fanout nodes of any path passing through q. Therefore, this does not qualify either as a hazard-free propagation or quality constriant. **Hence, like $d1$, even if we compute delay tests that satisfy both the hazard-free propagation constraints and quality constraints it is not guaranteed to detect this defect.**

Once again note that no stuck-at tests for q is guaranteed to set h, k to 1. Therefore, **no transition test for q rising will detect this defect**.

Next consider defect $d3$ of Figure 8(a) where the gates of both P1, N1 are joined and open from the rest of the circuit. In this case the two transistors are usually in a conducting state and conducts rather strongly. If pullup strength of $P1$ is much stronger than the pulldown strengths of both $N1, N2$ then setting both k, h to 1 will not set p to 0 and hence the fault can be detected as a stuck-at 1 fault during logic testing. This is usually not the case and p will be at an intermediate voltage on a pplication of a vector that either sets both h, k to

1 or h, k to 1, 0. This causes a slow-to-fall transition at s in response to a rising transition at q. Thus, it can be detected by any path delay fault test-pair that detects defect $d1$. The test-pair of Figure 8(c) is one such test-pair. **Once again, the reader can verify that even if we compute delay tests that satisfy both the hazard-free propagation and the quality constraints it is not guaranteed to detect this defect because constraints on h,k has to be satisfied**.

4.2 Open Output

(i) Large opens. Consider defect $d1$ of Figure 9(a)whose gate level circuit is shown in Figure 9(b). In this case all the transistors $P1, N1, P3, N3$ conduct strongly.

If $P1$ ($P3$) has a much larger pullup strength than $N1, N2$ ($N3, N4$) then logic testing will detect it as a h stuck-at 1 (k stuck-at 1). It may also manifest itself as both h stuck-at 1 and k stuck-at 1.

Note that if the pullup strength of $P1$ ($P3$) is not much larger than $N1, N2$ ($N3, N4$) then we have a weak 1 at h (k). This, under certain conditions, delays the falling and rising transition at m. Let us again consider how a test-pair $< T1, T2 >$ can detect such a defect during delay testing. Both $T1, T2$ sets g to 1 ensuring that k is set to a weak 1 during the entire interval, in the presence of the defect. In addition, $T1, T2$ should create a rising transition at h which causes a slow-to-fall transition at m. One such test-pair is shown in Figure 9(b).

This is an interesting example for the following reason. The test-pair detects the delay caused by a defect that delays the propagation of a falling transition at a along paths $< a, e, h, m >$, $< a, f, h, m >$. **However, the test-pair is not a hazard-free robust test-pair for input falling for either of the two paths**.

(ii) Narrow opens. For such defects if given sufficient time the floating gates will acquire the correct voltage. Hence the static logic behaviour is not affected. Therfore, logic testing cannot detect such defects. They however affect the dynamic logic behaviour. Next, let us investigate how a test-pair $< T1, T2 >$ can detect such defect during delay-testing. Both $T1, T2$ sets e to 0 thereby ensuring that h is set to 1 during the entire duration. Let $T1$ set g to 0 thereby ensuring that the value at k after application of $T1$ is 1. Let $T1$ also set f to 0 so that the gates of $P3, N3$ are discharged to a value close to 0. This will cut-off $N3$

and turn-on $P3$. Next, $T2$ switches both g, f to 1. Since the open conducts a small leakage current the falling transition at k will be delayed. It can be verified from Figure 9(c) that a test-pair that satisfies all these constraints is $< a = S1, b = f, c = S1, d = f >$. It will therefore detect the defect.

This example is interesting because the constraint required transitions at two different inputs f, g of a gate. **Satisfaction of such constraints is not required by any SPP-hazard free robust delay tests for path delay faults**. MPP-hazard free robust tests for any fault that causes both f, g to rise is not guaranteed to set e to $S0$. Hence, MPP hazard free robust tests are not guaranteed to detect this defect.

5 Delay Tests and Bridges

Two kinds of resistive bridges viz. external and intra-gate bridges are considered. Three kind of intra-gate defects viz. gate-source, gate-drain and source-drain bridges are considered.

External. Refer to $d1$ of Figure 10(a) for an example. If the bridge resistance is small then is causes a faulty static logic behaviour. Assume that the bridge resistance is large. In this case the defect is unlikely to be detected during logic testing. However, it can be detected during delay testing. A test-pair for such a defect should activate the defect by setting g to an intermediate voltage. This causes the transistor-pair in gate H driven by g to conduct weakly and leads to the delay fault $< d, h >_r$. To activate this path delay fault the test-pair $< T1, T2 >$ should be such that either: $T2(e) = 1, T2(g) = 0$; or $T2(e) = 0$, $T2(g) = 1$. This constraint is such that: e is neither an off-path input nor a side fanout node; and the test-pair cannot satify the hazard-free propagation property. Hence, **no hazard-free robust delay tests detects this defect !!**

Source Drain. Refer to defect $d2$ of Figure 10(b) for an example. The corresponding gate level circuit is shown in Figure 10(c). If the bridge resistance is small it causes a change in the static logic behaviour of the circuit. Assume that the bridge resistance is large. In this case the defect is unlikely to be detected during logic testing. However, it can be detected during delay testing provided $T2$ of the test-pair $< T1, T2 >$ sets d to a weak 1. This activates the path delay fault $< c, e >_r$. Thus, to activate the defect the test-pair for $< c, e >_r$ must satisfy the following constraints $T2(b) = 1, T2(a) = 0$.

Since a is neither an off-path input nor a side fanout node of $< c, e >$ these constraints on the test-pair do not qualify either as a hazard-free propagating or quality constraint. **Hence, no hazard-free robust test-pair for path delay faults can guarantee the detection of this defect**.

Gate Source. Refer to defect $d3$ of Figure 10(d) for an example. The corresponding gate level circuit is shown in Figure 10(e). For small bridge resistance the defects cause a faulty static logic behaviour of the circuit. Assume that the bridge resistance is large. In this case the defect is unlikely to be detected during logic testing. However, if e is set to an intermediate value due to the defect then it activates a $< d, h >_r$ path delay fault. To activate the defect the test-pair should be such that the second vector should set both e, c to 1. The reader can verify that **this constraint is such that it does not qualify either as a hazard-free propagation constraint or a quality constraint**. Hence, **hazard-free robust test-pairs for path delay faults are not guaranteed to detect such defects**.

Gate Drain. Such defects are very similar to gate source defects. We leave it to the interested reader to construct examples showing that for small resistances such defects are often detected by stuck-at tests. On the other hand, for large bridge resistance, even though it affects circuit delays current delay test generators are not guaranteed to compute tests to detect such defects.

6 Discussion

It was known for sometime that constraints, in addition to those for stuck-at faults, had to be satisfied to activate bridging faults. For sake of completeness refer to defect $d1$ of Figure 10(a) for an example. If the bridge resistance is small then it affects the static logic behaviour of circuits. In this case if T is such that in the fault-free case $T(e) = 0, T(g) = 1$ then the value at e in the faulty circuit will be a weak 1. Hence, it may be detectable during logic testing by a test for e stuck-at 1. However, note that not every test T for e stuck-at 1 detects this defect since T must satisfy the constraint that $T(a) = 1, T(b) = 1, T(c) = 0$. This is an example of **defect sensitization**. There are a number of tests for e stuck-at 1 viz. $< a = 1, b = 1, c = 1, d = 1 >$ that will not activate this defect and hence will not detect it. The fault can also be activated by setting e to 1 and b to 0. The fault may be detectable as g stuck-at 1. The test $< b = c = 1, a = 0, d = 1 >$ for g stuck-at 1 detects it but $< a = b = c = d = 1 >$ does not. Thus, **defects that cause faulty static logic behaviour are not guaranteed to be detected by tests for stuck-at faults**.

The implication of the above fact and the new facts unravelled in the previous sections can be summarized as follows.

- Firstly, there is a need to reasses methods that are used to compute logic tests. The method based on stuck-at faults is clearly lacking and there is a need for a new approach to compute logic tests.

- Transition tests and Delay tests for path delay faults are inadequate to detect defects that cause faulty dynamic logic behaviour. A new approach to computing atspeed tests is required.

- I_{DDQ} testing[5] detects many of the defects which, as the above facts suggests, may not be detected during logic testing or at-speed testing. This gives another reason to consider I_{DDQ} testing among the suite of test techniques that are used.

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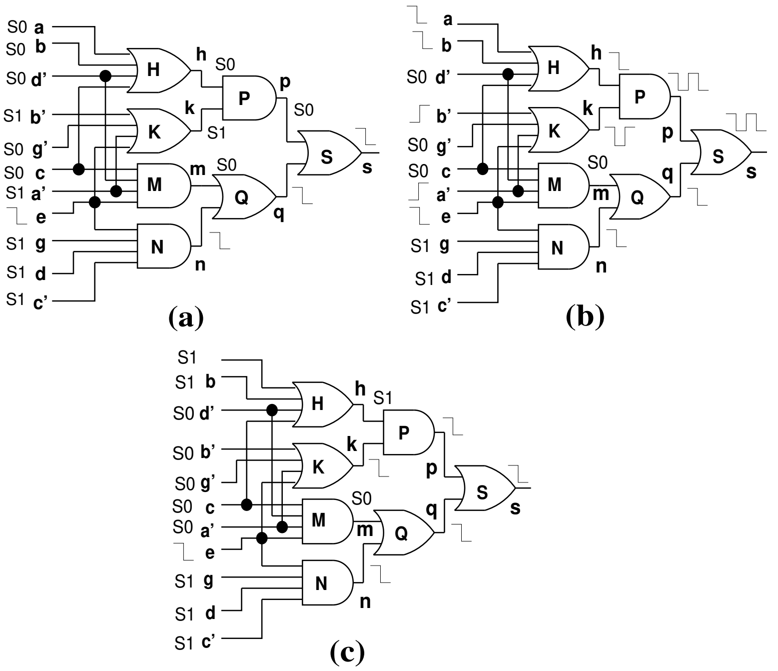

Figure 1: Illustration of different kinds of delay test-pairs

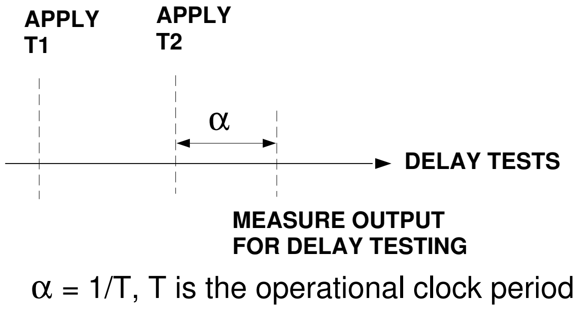

Figure 2: Timings for application of test-pairs

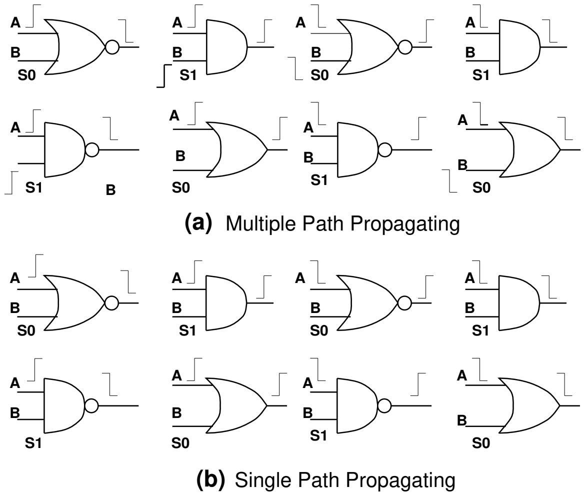

Figure 3: Definition of multiple, single path propagating hazard-free robust test-pairs

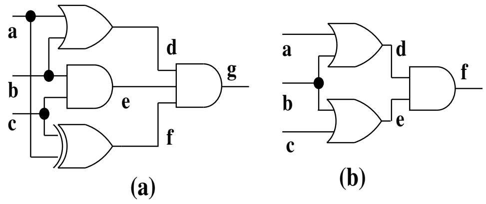

Figure 4: Example illustrating the advantage of using multiple path propagating robust test-pairs

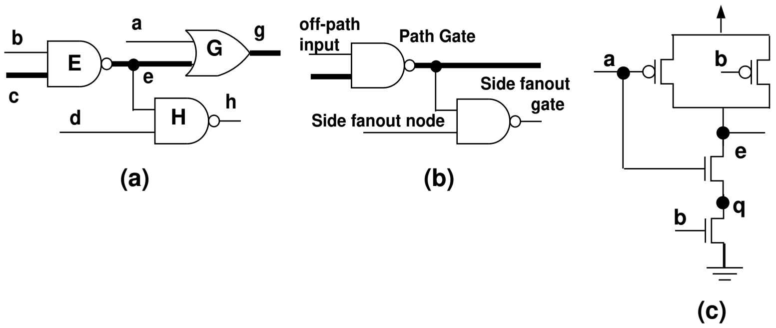

Figure 5: Quality of Robust Test-Pairs

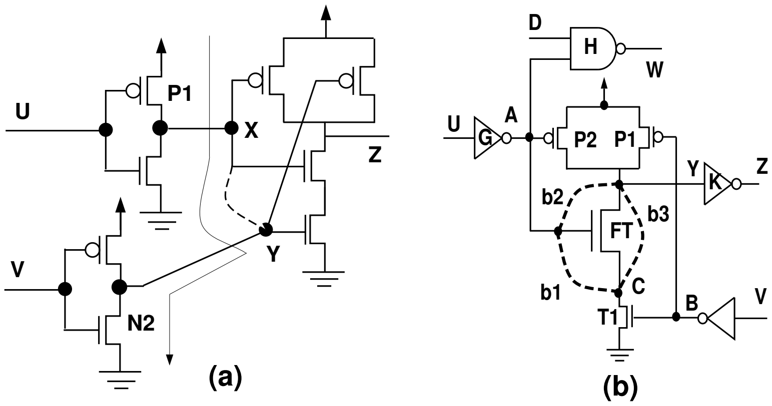

Figure 6: Impact of Shorts on Logic Behaviour

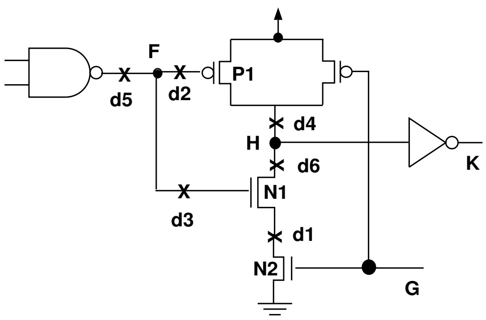

Figure 7: Impact of Opens on Logic Behaviour

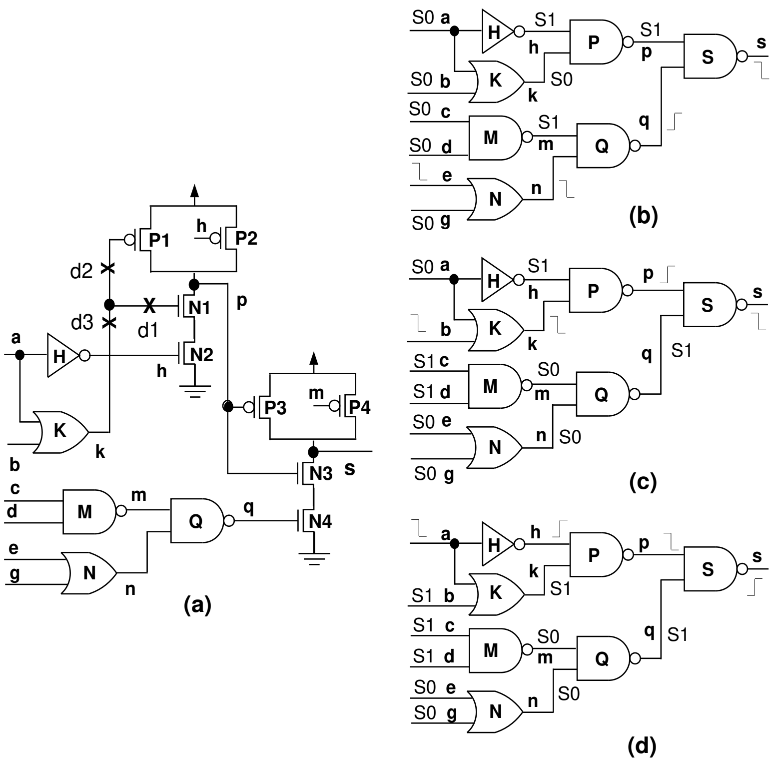

Figure 8: Delay tests to detect gate opens

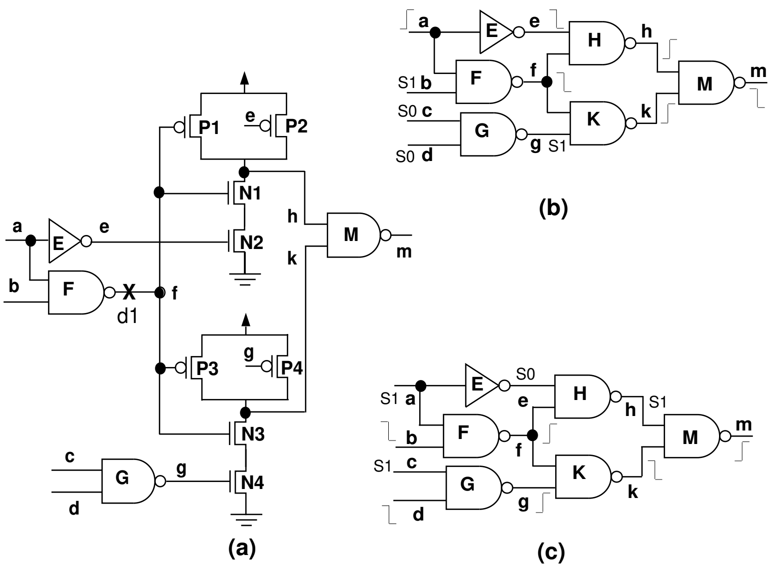

Figure 9: Delay tests to detect output opens

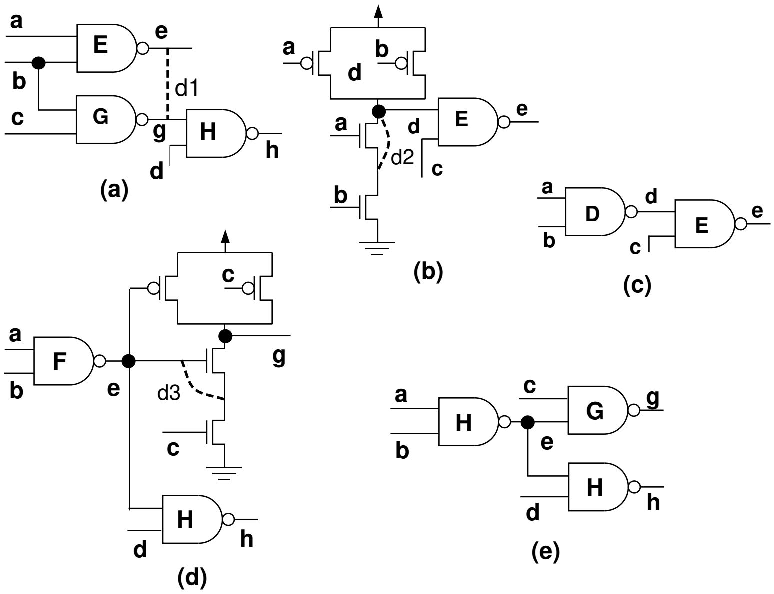

Figure 10: Delay tests to detect bridges