Minimizing Power Dissipation in Scan Circuits During Test Application *

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Abstract

Motivation for reducing power dissipation during test application is presented. A scheme for reducing power dissipation during test application, when scan test structure is used, is proposed. Algorithms required to exploit the proposed technique are discussed. Experimental results are presented.

keywords: Power dissipation, Full Isolated Scan, Full Integrated Scan.

1. Introduction

Growing size of VLSI circuits, along with the high transistor density, is making minimization of power dissipation an important issue in VLSI design. Power dissipation issues are addressed at various stages of circuit design. For example, circuits are synthesized so that average switching activity is reduced [1, 2, 3], technology mapping can be targeted for low power dissipation [4, 5], and physical design can be targeted for low power dissipation [6]. Power dissipation issues during test application must also be addressed. The motivation for this is discussed in section 2. Except for [7], we are unaware of any work that addresses power dissipation concern during testing. In [7] scheduling tests to minimize power dissipation in circuits containing BIST hardware is discussed. In this paper we address this problem for two different scan test structures viz. *Full Isolated Scan, Full Integrated Scan* [8]. These test structures are discussed in Section 4 wherein we also discuss how to account for all the power that is dissipated during test application when tests are applied using these test structures. Before that, in section 3, we discuss models for accounting for power dissipation. This model, which is the prevalent model in use for static CMOS circuits, is significantly different from the power dissipation model used in [7]. In our solution, as in [7], we impose the constraint that the test set not be modified so as to reduce fault coverage.

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By means of an example, in section 4, we show that for scan circuits power dissipation during test is a function of two parameters: the order in which the tests are applied; and the order in which the scan F/Fs are chained to form the shift register.

Computing the optimal order both for the scan flip-flops and the input vectors is an intractable problem. We therefore break up the problem into two subproblems: Test Vector Ordering; and Scan Latch Ordering. Problems are formally stated in section 5. As we will see in section 6, both these problems are themselves intractable. We are in the process of developing heuristics for these problems. In this paper we restrict ourselves to the heuristic for the first problem. Preliminary experimental results of these algorithms are provided in section 7. They are quite encouraging.

2. Motivation

To understand the reason for this we briefly discuss the stages a die passes through during its life span [9]. Broadly speaking they are: (a) The dies are etched on the wafer; (b) The dies are tested and cut out from the wafer; (c) The defective dies are removed and the good ones are packaged. After that a burn-in test is performed; (d) A percentage of the chips are tested. The defective ICs are identified; (e) The good chips are used in a system developed by the end user.

These stages differ in their ability to dissipate the power generated in the die as its inputs change state. In stage (b) the bare die has very little provision for power dissipation. In stages (c) and (d), the packaging can dissipate a significantly larger amount of power. In fact, the packaging used depends upon the amount of power that needs to be dissipated. In stage E, where the die will be used for most of its lifetime, additional provisions like heat dissipating fins etc. are provided.

During stage (b), because of the lower capability of the environment to dissipate power, test application stresses the die much more than any other stage. Thus, some of the bare die that escaped manufacturing defect, due to this additional stress, may fail during this test session. This reduces the die-yield (which is the ratio of the good dies available for packaging to the total number of dies etched) and hence the IC cost. In conjunction with other attempts to improve die-yield attempts should be made to reduce power dissipation during testing. Reduction in die-yield may not be significant for small, low density circuits. However, for larger and higher density circuits, as is the case for multichip modules, the problem is much more significant.

Another issue, in the context of power dissipation during test application, is that the possible sequences of input vectors applied during test is often a much larger super set of the possible sequences applied during its normal use. This is a consequence of the test structures embedded in the circuit. For example, if the circuit contains scan structures then during testing the latches can be set to encodings of unreachable states. Thus, during testing, sequences that lead to much larger power generation are often applied to the IC when compared with sequences that are applied during its normal use. A solution to this is to estimate the higher power generated during testing and provide the packaging for this higher value. This increases packaging cost and should be avoided as far as possible. Reducing power dissipated during testing is the other alternative.

The excessive power generated during testing, over and above the amount generated during its normal use, also affects system reliability. Systems are often tested at periodic intervals. During these periodic test sessions the IC is cycled through a higher stress level. This degrades its reliability and consequently that of the system. Attempts to reduce power dissipation during test application is also relevant in this context.

Tester cost is another concern. Excessive power dissipated during testing also requires power supplies that can source this elevated power requirement. For larger and higher density chips a given tester may fail to provide the required power. Rather than procuring a new tester, at an enormous cost, so as to meet the power requirement attempts should first be made to reduce the power dissipation during testing. Similar power supply constraints have also to be taken into account for battery powered systems that may not be able to supply adequate power during periodic system testing. Such systems are in wide spread use in portable computing systems, portable communication systems which are used extensively.

Thus, whether we are interested in improving die-yield, chip-yield, IC cost or system reliability we ought be concerned with the power requirements during testing and attempt to reduce it.

3. Power Dissipation Model

The two components of power dissipated in a CMOS circuit [10] are: Static dissipation due to leakage current or other current drawn continuously from the power supply (P_{st}) and dynamic dissipation due to (i) switching transient current (P_{sc}) and (ii) charging and discharging of load capacitances (P_d). The total power dissipation P_{total} is given by :- $P_{total} = P_{st} + P_d + P_{sc}$. As in [1] P_{st} and P_{sc} are neglected.

P_d is power required to charge and discharge the output capacitive load of every gate. P_d is approximated as follows: (1) $P_d = 1/2 \times C \times V_{DD}^2 \times N_G \times f$; where C = output capacitance; N_G = total number of gate output transitions ($1 \rightarrow 0$ or $0 \rightarrow 1$); and f = repetition frequency.

Equation (1) implies that power is dissipated at a node when the input vector is changed from T_i to T_{i+1}. Let $P_{i,i+1}$ be the total power dissipated in the circuit when inputs change from T_i to T_{i+1}. Then,

$$P_{i,i+1} = \sum_{j \in SetofNodes} 1/2 \times C_j \times V_{DD}^2 \times N_{G_j} \times f \qquad (2)$$

Thus power dissipated at a node is proportional to the number of transitions (N_{G_j}) at that node. This depends on the gate delays and sequence of input vectors applied. Next we discuss how to compute the the transitions at the other nodes.

Under the zero-delay model, all gates are assumed to have zero delay. The four possible transitions and the corresponding logic levels are : static-zero (s0) $\Rightarrow$ Logic level remains zero; static-one (s1) $\Rightarrow$ Logic level remains one; rising (r) $\Rightarrow$ Logic level changes from 0 to 1; falling (f) $\Rightarrow$ Logic level changes from 1 to 0. For example for a two-input AND gate output behavior under zero-delay model is described using Table 1.

In the General-Delay model, gates can have arbitrary delays. The six valued logic adequately describes the signal state at a line on application of an input pair $\langle T1, T2 \rangle$. They are: s0 and s1 as described above; hazard-rising (hr) $\Rightarrow$ Initial logic level 0, final logic level 1 and one or more transitions; hazard-falling (hf) $\Rightarrow$ Initial logic level 1, final logic level and one or more transitions; hazard-0 (h0) $\Rightarrow$ hazard with initial and final logic level 0; hazard-1 (h1) $\Rightarrow$ hazard with initial and final logic level 1.

Let GDV = $\{$s0, s1, hr, hf, h0, h1$\}$. Note that any state of the line, with any number of glitches during transitions, can be uniquely represented by an ordered pair $\{(a, b) : a \in I \text{ and } b \in GDV\}$, where a denotes number of glitches during transitions. Transitions ($0 \rightarrow 1 \rightarrow 0 \rightarrow 1$) is represented as (3,hr) while transitions ($1 \rightarrow 0 \rightarrow 1 \rightarrow 0 \rightarrow 1$) is represented as (4,h1). As an example two-input AND gate output behavior under general-delay model is described by Table 2.

Let M be any memory element. Let M_{min} denote the number of gate level transitions occurring within M for the input changes $0 \rightarrow 0$ or $1 \rightarrow 1$. Similarly, let M_{max} denote the number of transitions for input changes $1 \rightarrow 0$ or $0 \rightarrow 1$. e.g. under zero delay model, for the D-FF shown in Figure 1(a), $M_{min} = 1$ and $M_{max} = 4$. Similarly for the latch shown in Figure 1(b) $M_{min} = 2$ and $M_{max} = 6$.

Thus, by traversing a given combinational network in a topological order, the number of transitions can be computed using the above tables and the value of M_{min} and M_{max} in linear time.

4. Scan Structures

Block diagram of Full Isolated Scan is shown in Figure 2(a) [8]. R' is the system register and R_s is the test register where the tests are scanned in serially. A test vector is loaded into R_s in N clock cycles where N is the number of F/Fs in the scan chain. In cycle $N + 1$ contents of R_s are transferred to R' and applied to the combinational circuit C. In cycle $N + 2$ a part of the output of C is latched into R'. In cycle $N + 3$ the contents of R' are transferred to R_s. During the next N cycles the output response is scanned out while the next input vector is scanned in. This scan technique is different from Full Integrated Scan [8] where, as shown in Figure 2(b), R_s, R' are merged to form one register R_s. In Full

Isolated Scan, unlike Full Integrated Scan, as a new vector is scanned into R_s the state of R', i.e. the inputs to the combinational circuit C, is not changed[8] .

To account for power dissipation in Full Isolated Scan assume the response to T_1 is in R_s, T_2 is to be scanned in and the response of T_1 to be scanned out. Power dissipated from this clock cycle to the clock cycle in which the response of T_2 is loaded into R_s i.e. $\underline{Interval(T_1, T_2)}$ can be broken down as follows.

(a) For the first N clock cycles power is dissipated in R_s as T_2 is scanned in and the response from T_1 is scanned out.

(b) In cycle $N+1$ power is dissipated in R' as T_2 is transferred from R_s to R'. In this clock cycle power is also dissipated in the combinational circuit C as inputs to C change from the response of T_1 to the new vector T_2. The assumption here is that during the initial part of the cycle the state of R' changes. During the rest of the cycle transitions in C can occur.

(c) In cycle $N+2$ power is dissipated in R' as the response of C to T_2 is latched onto R'. In this cycle, power is also dissipated in C as the inputs to C changes from T_2 to an intermediate vector T_2'. T_2' is defined as follows. Let I be the primary inputs of C and I' be the outputs of R' driving C. Then, $T_2'(x) = T_2(x), \forall x \in I$ and $T_2'(y) = T_2(Y), \forall y \in I'$ where Y is the output of C corresponding to the state variable y. For example, in Figure 3 assume that $T_2 = \langle X1 = 1, y1 = 0, y2 = 1, y3 = 0\rangle$. Then, $T_2' = \langle X1 = 1, y1 = 1, y2 = 1, y3 = 1\rangle$.

(d) In cycle $N+3$ power is dissipated in R_s as the response of C on application of T_2 is transferred to R_s.

The above process is repeated for the entire sequence. See Figure 3. Let x_1 be its primary input, $F = \{F_1, F_2, F_3\}$ be the scan F/Fs, and $S = \{S1, S2, S3\}$ the system F/Fs. Assume the F/Fs to be chained as shown in Figure 1(b). Let y_i denote the present state and Y_i denote the next state for flip-flop F_i. We represent an input vector of C as an ordered tuple of the values of x_1, y_1, y_2, y_3, in that order independent of the order in which the scan latches are chained. Assume simplicity we assume the zero-delay model; and the capacitance of each node to be equal to its fanout. Since the values of the constants $V_{DD}, \frac{1}{2}, f$ in Eqn (2) do not affect the final flip-flop and test vector orders that we compute we disregard them.

Let $T_1 = \langle 0000\rangle$ and $T_2 = \langle 1001\rangle$ and assume that the flip-flop order is $\langle F1, F2, F3\rangle$. We assume that the value of X_1 is updated when R' is updated. The state of each F/F, during the 6 clock cycles of $Interval(T_1, T_2)$, along with the power dissipated is shown in Table 3. The total power dissipated is 79. Table 4 shows the calculations for $Interval(T_2, T_1)$. The total power dissipated is 51.

To compute the total power dissipated, on application of the entire test set, we add up the power dissipated during each interval. We assume that: initially R_s, R' are set to the all zero state; and while the response of the last input vector is scanned out the all zero input is scanned in. This last $Interval$ requires three clock cycle for our example and N clock cycle in general. The clock cycles during which the first test vector T_i is scanned in and its response is latched onto R_s is denoted by $\underline{Interval(\#, T_i)}$. The last N clock cycles, during which the response of the last vector T_j is scanned out, is denoted by $\underline{Interval(T_j, \#)}$. The reader can verify that if the order in which the tests are applied is (T_1, T_2) ((T_2, T_1)) the total power dissipated is 109 (81). Thus, changing test vector order, keeping F/F order constant, affects total power dissipation.

Next, let us have a closer look at Tables 3, 4. During cycles 1, 2, 3 (in general 1 through N) the state of R' remains unchanged. Thus, there is no power dissipation in C, R'. However, power is dissipated in R_s. During the next two clock cycles power is dissipated only in C and R'. In the last cycle power is dissipated only in R_s.

If the flip-flop order is changed to $\langle F3, F1, F2\rangle$ then in Table 3, during the first three cycles the total power dissipated is 22 instead of 38. The power dissipated in the next three cycles will not change. *Thus, for* Full Isolated Scan*, power dissipated in the first N cycles of an* Interval *is a function of both the order of the test vectors and the order of the flip-flops. The power dissipated in the next 3 cycles is a function only of the order in which the vectors are applied.*

For *Full Integrated Scan* power is dissipated, in every clock cycle, both in R_s and C. Every $Interval$, except the last, now consist of $N+1$ clock cycles. Consider the circuit of Figure 3(b) and assume that: $T_1 = \langle 0100\rangle, T_2 = \langle 0101\rangle$; and the flip-flop order to be $\langle F1, F2, F3\rangle$. From Table 5 (6) we see that the total power dissipated during $Interval(T_1, T_2)$ ($Interval(T_2, T_1)$) is 51 (36). If we change the flip-flop order to $\langle F1, F3, F2\rangle$ Table 7 implies that power dissipated during $Interval(T_1, T_2)$ is 59.

5. Problem Definitions

We state the problems in this section. Please refer to the appendix for the derivations of expressions used in this section.

(1)(a) **OPT_SEQ_TOTAL (OST):** Given a combinational circuit C and a set of input vectors $T = \{t^1, ..., t^l\}$. Compute an optimal input sequence $\langle r^1, ..., r^l\rangle$ of T s.t. P_v^{total}, defined below is minimized.

$$P_v^{total}(\#, r^1) + \sum_{i=1}^{l-1} P_v^{total}(r^i, r^{(i+1)}) + P_v^{total}(r^l, \#)$$

$P_v^{total}(r^i, r^{(i+1)})$ is the total power dissipated during $Interval(r^i, r^{(i+1)})$. A sequence with the best average power dissipation can be obtained using the solution to OST. Note that in these problems, we do not estimate the power dissipation but compute an ordering of a given test set of input vectors such that power dissipation is minimized. As stated in section 3, given the library modules and the number of transitions for each pair of input vectors, estimation of the power dissipation in the circuit can be obtained by using equation (2) and solutions to these problems.

(1)(b) **OPT_SEQ_PEAK (OSP)**: is similar to OST except we now minimize the following expression for P_v^{max} .

$$\max\{P_v^{max}(\#, r_1), \max_{i=1}^{l-1} P_v^{max}(r^i, r^{(i+1)}), P_v^{max}(r_l, \#)\}$$

(2)(a) **FF_REORDER_TOTAL (FRT) :** Given a sequential circuit Q with set of memory elements $F = \{f^1, \ldots, f^m\}$, test set T, find an ordering $S = \{r^1, \ldots, r^m\}$ of F such that

$$P_s^{total} = P_s^{total}(\#, r^1) + \sum_{i=1}^{l-1} P_s^{total}(r^i, r^{(i+1)}) + P_s^{total}(r^l, \#) \text{ is minimized.}$$

(2)(b) **FF_REORDER_PEAK (FRP) :** is similar to FRT except that maximum instead of total power dissipation during scan is minimized.

$$P_s^{max} = \max\{P_s^{max}(\#, r^1), \max_{i=1}^{l-1} P_s^{max}(r^i, r^{(i+1)}), P_r^{max}(r^l, \#)\}$$

6. Hardness Results and Construction of Transition Graph

6.1 Hardness Results

Following theorems give the hardness of OSP and OST for Full Isolated Scan. Note that the proofs are independent of the delay model used. We use Hamiltonian Path (HP) Problem to prove that OSP is NP-Hard. HP is defined as follows:

HP: Given an undirected graph $G = (V, E)$, where $V = \{v_1, \ldots, v_n\}$, find path $\langle v_{i_1}, v_{i_2}, \ldots, v_{i_n}\rangle$ s.t. $i_j \in \{1, \ldots, n\}\ \forall j.$ and every node in the graph is visited once and only once

Theorem 6.1 *OSP is NP-hard.*

Proof: HP for an undirected graph is known to be NP-Hard [11]. We reduce HP to OSP. Let $G = (V, E)$ be any undirected graph where $V = \{v_1, v_2, ..., v_n\}, E = \{e_1, e_2, ..., e_m\}$, $n = \mid V \mid$, $m = \mid E \mid$. We construct the following instance of OSP with circuit Q and test set T. Q consists of the combinational part C and two registers R' and R_s. C consists of $(n-1)m$ 2-input OR gates. Inputs of each OR gate are tied together. Thus there are $(n-1)m$ inputs and $(n-1)m$ outputs. All the inputs and outputs are connected to the register R'. Hence there are no primary inputs to circuit Q.

Input set T consists of n input vectors $T = \{t^1, ..., t^n\}$. Each input vector corresponds to a node in G. Every input vector has m parts, one for each edge and each part has $n-1$ bits. Thus each vector t^i consists of $(n-1)m$ bits.

Let $t^i(j)$ = j^{th} part of t^i and let $e_j = (v_a, v_b)$ s.t. $1 \leq a < b \leq n$.

$$t^i(j) = \begin{cases} 10^{n-2} & \text{if } i = a \text{ or } i = b \\ 0^i 10^{n-1-(i+1)} & \text{if } i < a \\ 0^{i-1} 10^{n-1-i} & \text{if } a < i < b \\ 0^{i-2} 10^{n-i} & \text{if } i > b \end{cases}$$

For example, consider the graph shown in Figure 5(a). The circuit C and input set corresponding to this graph is shown in Figure 5(b) and Table 8 respectively.

We next show that G is hamiltonian iff minimum of P_{max} for the circuit C and test vector set T is $(12 \times (e-1) + 2 \times [(e-1) \times (n-3) + (n-1)])$. If edge $(v_i, v_j) \in E$ then $P_{max}(t^i, t^j) = \max\{R'(t^i_n, t^j_p), C(t'^i, t^j)\}$. Here, $R'(t^i_n, t^j_p) = 2 \times (e-1) \times M_{max} + [(e-1) \times (n-3) + (n-1)] \times M_{min}$. Assuming $M_{min} = 2$ and $M_{max} = 6$, we get $R'(t^i_n, t^j_p) = 12 \times (e-1) + 2 \times [(e-1) \times (n-3) + (n-1)]$. $C(t'^i, t^j) = 2 \times (e-1)$. So $P_{max}(t^i, t^j) = 12 \times (e-1) + 2 \times [(e-1) \times (n-3) + (n-1)]$. It can be verified that if edge $(v_i, v_j) \notin E$, then $P_{max}(t^i, t^j) = 12 \times e + 2 \times e \times (n-3)$. Therefore min $P_{max} = (12 \times (e-1) + 2 \times [(e-1) \times (n-3) + (n-1)]) \Rightarrow \exists$ a input sequence $\langle t^{i_1}, ..., t^{i_n} \rangle$ such that for all k, $(v_{i_k}, v_{i_{k+1}}) \in E$. This implies that $\langle v_{i_1}, ..., v_{i_n} \rangle$ is a hamiltonian path in G. Thus G is hamiltonian.

Conversely, assume that G is hamiltonian. Let $\langle v_{i_1}, ..., v_{i_n} \rangle$ be the HP. We schedule input vectors $\langle t^{i_1}, ..., t^{i_n} \rangle$. Now $(v_{i_k}, v_{i_{k+1}}) \in E$ hence $P_{i_{k,k+1}} = (12 \times (e-1) + 2 \times [(e-1) \times (n-3) + (n-1)])\ \forall k \in \{1, ..., n-1\}$. Hence P_{max} for the given path is $(12 \times (e-1) + 2 \times [(e-1) \times (n-3) + (n-1)])$. Note that this P_{max} will be minimum because for every sequence $P_{max} = (12 \times (e-1) + 2 \times [(e-1) \times (n-3) + (n-1)])$ or $(12 \times e + 2 \times e \times (n-3))$ as argued above. Hence the proof. □

Theorem 6.2 *OST is NP-hard.*

Proof: Using the same construction as in the proof of Theorem 6.1, it can be verified that graph G is hamiltonian iff sum of the output transitions in a sequence is $(n-1) \times (12 \times e + 2 \times e \times (n-3))$. □

6.2 Flip flop ordering

We show that FRP is NP-Hard under zero delay model.

Theorem 6.3 FRP *is NP-Hard.*

Proof: We reduce HP to FRP. Let the given instance of HP be $G = (V, E)$ where: $V = \{v_1, \ldots, v_n\}$, $E = \{e_1, \ldots, e_m\}$, $\mid V \mid$ = n, $\mid E \mid$ = m. We construct an instance of FRP where: C is the given circuit, S_1 is the scan-in vector set and S_2 is the scan-out vector set. Next C, S_1, S_2 are defined. The circuit C consists of n two-input OR gates, one for each node v in G. Let G_i be the gate corresponding to node

v_i. Each of the these OR-gates is driven by an input variable. Gate G_i is driven by x_i. These input variables are the output of the scan flip flops. Let x_i be the output of flip flop F_i. We have to reorder these flip flops.

By construction S_1 will be the same as S_2. We next define S_1. S_1 consists of $t = 2(n-1)m$ vectors and they are ordered as $\langle T_1, \ldots, T_t \rangle$. Each T_j has n-bits (corresponding to the number of nodes). Let T_i^j be the bit of T_i which will be the output of F_j. We next define each of the T_i's.

In order to define the T_i's we define a table consisting of n rows $r_1, \ldots, r_n$ and t columns. Column i defines T_i. We next define each row.

Every row is partitioned into m parts corresponding to the m edges in the graph G. Let r_i^j denote the portion of row r_i corresponding to edge e_j where $e_j = (v_a, v_b)$. Each r_i^j has $2(n-1)$ entries defined as follows.

$$r_i^j = \begin{cases} (01)(00)^{n-2} & \text{if } i = a \text{ or } i = b \\ (00)^i(01)(00)^{n-1-(i+1)} & \text{if } i < a \\ (00)^{i-1}(01)(00)^{n-1-i} & \text{if } a < i < b \\ (00)^{i-2}(01)(00)^{n-i} & \text{if } i > b \end{cases}$$

For example, for the graph shown in Figure 6 the scan-in vectors are shown in Table 9. Each column of the table represents a scan-in vector corresponding to the scan chain $R = \langle f_a, f_b, f_c, f_d \rangle$, e.g. the first vector is 0000 , the second one is 1100 and so on. Since the scan-in and scan-out vectors are same, each bit (or pair of bits) passes through all the flip-flops. So for the scan chain R, sequence of bits scanned-in are 0000 1100 0000. . . . For any ordered pair of flip-flops $\langle f_i, f_j \rangle$ two cases need to be considered to compute the number of transitions :- (1) when f_i is not the last flip-flop in the scan chain (2) when f_i is the last flip-flop and f_j is the first flip-flop in the scan chain. In case (1), the number of transitions can be computed by XORing the vectors corresponding to f_i and f_j, e.g. for the scan chain R and for the ordered pair $\langle f_a, f_b \rangle$ number of transitions = $r_a \oplus r_b$. In case (2), the number of transitions are obtained by multiplying the vector r_i by 2 (i.e. shifting to the right by one bit) and XORing it with r_j, e.g. for the scan chain R and the flip-flop ordering $\langle f_d, f_a \rangle$, number of inter-vector transitions is given by $(2 \times r_d) \oplus r_a$.

Next we show that graph G has a hamiltonian path iff there exists a scan chain for which the total number of transitions during scan-in and scan-out process are $(2 \times (m-1) \times (n-1)) + 2 \times m$. In case (1) discussed above, an edge $(v_a, v_b) \Rightarrow$ XOR(r_a, r_b) = $2(m-1)$. No edge between $(v_a, v_b) \Rightarrow$ XOR(r_a, r_b) = $2m$. In case (2), XOR(r_a, r_b) = $2m$ irrespective of whether an edge between (v_a, v_b) exists. If G has a hamiltonian path, then the total number of transitions = $2(m-1) \times (n-1) + 2m$. Conversely, if the total number of transitions = $2(m-1) \times (n-1) + 2m$ then there must be a sequence of flip-flops $\langle f_{i_1}, \ldots, f_{i_n} \rangle$ such that $(v_{i_k}, v_{i_{(k+1)}}) \in E \; \forall k = 1, \ldots, n-1$. i.e. G contains a hamiltonian path. Hence the proof. □

6.3 Construction of Transition Graph

Since OSP and OST are NP-Hard, one has to resort to heuristics which yield near-optimal solutions. All the heuristics will reduce the given problem to *path traversal problems* in a directed graph. The edge weights and node weights are assigned using the functions defined below. The directed graph constructed for OST is *Total Transitions Graph (TTG)*. Next, we show how to compute TTG for Full Isolated Scan given an instance of OST.

Let the test set be $\{t^1, \ldots, t^n\}$, the multilevel sequential circuit Q consist of a combinational part C, system and test registers R' and R_s respectively. $TTG = (V', E)$ is a complete directed graph s.t. $V' = V \cup \{v_0, v_{n+1}\}$ and $V = \{v_1, \ldots, v_n\}$. Here v_0 (v_{n+1}) represents a node corresponding to start (end) of the test sequence and each $v_i \in V$ corresponds to a test vector t^i. We define two weight functions $w_1^{max} : E \to I$ and $w_2^{max} : V' \to I$; for computing the edge weights and the node weights of TTG respectively. For an edge (v_i, v_j), $w_1^{total}(v_i, v_j) = R'(t_n^i, t_p^j) + C(t'^i, t^j)$. Let G_l denote output capacitance of node l in the combinational circuit C and let $w_l(v_i, v_j)$ denote the number of transitions at node l when t^j is applied after t'^i, then $C(t'^i, t^j) = \sum_{l \in L} G_l \times w_l(i, j)$. $R'(t_n^i, t_p^j)$ can be computed from equation (5). Please see appendix. For a node v_i, $w_2^{total}(i) = C(t^j, t'^j) + R'(t_p^j, t_n^j) + R_s(t_p^j, t_n^j)$. $w_1^{total}(v_0, v_i) = R'(\#, t_p^i) + C(\#, t^i)$. $w_1^{total}(v_i, v_{n+1}) = R'(t_n^i, \#) + C(t'^i, \#)$. Thus OST can be restated as: Find a hamiltonian path $\langle v_{i_0}, \ldots, v_{i_n}\rangle$ in TTG s.t. $\sum w_1^{total}(i_k, i_{k+1})$ for k = 0,. . . , n is minimized. A *Maximum Transitions Graph (MTG)* can be defined similarly and OSP can be restated as a Traveling Salesman Problem on MTG where maximum of the edge weights is to be minimized. Similarly, TTG and MTG can be constructed for Full Integrated Scan using derivations given in the appendix.

Consider the circuit in Figure 3(a). Consider a test set $T = \{t^1 = 0000, t^2 = 1001, t^3 = 0100, t^4 = 0010\}$ for this circuit. Let each vector t^i be represented as x_1, y_1, y_2, y_3. $w_1^{total}(i, j)$ for each edge (i, j) is represented in TTG; see Figure 4. . Similarly, w_2^{total} for each node i is represented. It can be verified that total power dissipation for the sequence $\langle s, t^1, t^2, t^3, t^4, t\rangle$ is 108. For the sequence $\langle s, t^4, t^2, t^1, t^3, t\rangle$, it is 122.

In the following sections we describe the heuristics and experimental results for OST under both the delay models.

7. Heuristics and Experimental Results

Given a TTG we use the following simple greedy heuristic to find a traveling salesman tour.

GreedyATSP (TTG)

(0) Tour $\leftarrow \phi$

(1) Sort all the edges

(2) **while** (Tour not complete)

(3) $e \leftarrow$ pop an edge from the sorted list

(4) **if** (e can be added to Tour)

(5) Tour $\leftarrow$ Tour $\cup \{e\}$

(6) **end while**

If the graph has m edges then the algorithm runs in $O(mlogm)$ time. Experiments are performed for both the scan techniques viz. Full Isolated Scan and Full Integrated Scan using both zero and general delay models. Results are tabulated in Table 10, 11, 12 and 13. Columns initial trans and final trans represent the total transitions for the initial sequence and final sequence of test vectors. Percentage improvement is shown in the fourth column and user timings are given in the final column. Experiments were performed with ISCAS89 circuits on Sun SparcII machines. Test sets were generated using Combinational atpg tool ATALANTA [12].

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Appendix

We use following notation.

PI = $\{x_1, \ldots, x_n\}$ be the primary inputs of a sequential circuit Q

PS = $\{y_1, \ldots, y_n\}$ be the present state inputs of Q

NS = $\{Y_1, \ldots, Y_n\}$ be the next state outputs of Q

F = $\{f_1, \ldots, f_m\}$ be a set of FFs in Q

R = $\langle r_1, \ldots, r_m\rangle$ define a flip-flop ordering in scan-chain

t^i = $\langle x_1^i, \ldots, x_n^i, y_1^i, \ldots, y_m^i\rangle$ be a test vector,
where $\langle x_1^i, \ldots, x_n^i\rangle$ are primary inputs and
$\langle y_1^i, \ldots, y_m^i\rangle$ are present state variables

t_p^i = $\langle y_1^i, \ldots, y_m^i\rangle$ be the present state part of t^i

t_n^i = $\langle Y_1^i, \ldots, Y_m^i\rangle$ be the next state part of t^i

t'^i = $\langle x_1^i, \ldots, x_n^i, Y_1^i, \ldots, Y_m^i\rangle$ be a vector,

Full Isolated Scan

During Full Isolated Scan, let $I(t^i, t^j)$ denote an interval when (a) t_p^j is scanned in and t_n^i is scanned out in test register R_s ; (b) contents of R_s, t_p^j, are loaded into system register R' ; (c) result of the application of t^j to the combinational circuit C, t^j_n, is latched to R' and (d) R' is loaded into R_s. Let $I_s(t^i,t^j)$ denote the sub-interval of $I(t^i,t^j)$ when scan process i.e. (a) is performed. Let $I_v(t^i,t^j) = I(t^i,t^j) - I_s(t^i,t^j)$ be the remaining interval i.e. when (b), (c) and (d) are performed. Let $I(\#,t^i)$ denote an interval when t^i is the first test vector scanned in. Similarly, let $I(t^i,\#)$ denote an interval when t^i is the last test vector scanned out. As discussed in section 3, switching activity during $I(t^i,t^j)$ consists of the following terms. Switching activity

(i) in R_s during scan-in of t^j_p and scan-out of of t^i_n;

(ii) in R' during loading of t^j_p into R' when it contains t^i_n, say $R'(t^i_n,t^j_p)$;

(iii) in C due to input change from t^i to t^j, say $C(t^i,t^j)$;

(iv) in C due to input change from t^j to t'^j, say $C(t^j,t'^j)$;

(v) in R' due to latching t^j_n into R' when it contains t^j_p, say $R'(t^j_p,t^j_n)$;

(vi) in R_s due to loading t^j_n into R_s when it contains t^j_p, say $R_s(t^j_p,t^j_n)$.

Let $P_s(t^i,t^j)$ denote the switching activity during scan-in and scan-out process (i.e. during $I_s(t^i,t^j)$); let $P_v(t^i,t^j)$ denote switching activity duing rest of the interval in $I(t^i,t^j)$ (i.e. during $I_v(t^i,t^j)$). We first derive expressions for peak/total power dissipation during $I_s(t^i,t^j)$.

Switching Activity during $I_s(t^i,t^j)$: Let $S = \langle s_1,\ldots,s_{2m}\rangle = \langle Y^i_1,\ldots,Y^i_m,y^j_1,\ldots,y^j_m\rangle$ denote the scan-vector. Let $S(i:j)$ denote the subvector $\langle s_i,\ldots,s_j\rangle$. In the beginning of the scan-in process, register R_s contains $S(1:m) = \langle Y^i_1,\ldots,Y^i_m\rangle$. At the end of the scan process, R_s contains $S(m+1:2m) = \langle y^j_1,\ldots,y^j_m\rangle$. Before i^{th} clock cycle inputs to the flip-flops in R_s are $S(i:m+i-1)$; after i^{th} cycle they change to $S(i+1:m+i)$. If $p(i)$ denote number of 1's in $S(i:m+i-1)\oplus S(1+i:m+i)$, then switching activity during i^{th} clock cycle is denoted by $(p(i)\times M_{max} + (m-p(i))\times M_{min})$. Therefore, peak power and total power dissipation during $I_s(t^i,t^j)$, say $P^{max}_s(t^i,t^j)$, is given by :

$$P^{max}_s(t^i,t^j) = \max_{k=1}^{m}(p(k)\times M_{max} + (m-p(k))\times M_{min}) \quad (3)$$

$$P^{total}_s(t^i,t^j) = \sum_{k=1}^{m}(p(k)\times M_{max} + (m-p(k))\times M_{min}) \quad (4)$$

Note that the only part in equation (3) and (4) that depends on the sequence of the test vectors is the input change in flip-flops due to the difference in last bit of the vector t^i_n i.e. Y^i_m and first bit of the vector t^j_p i.e. y^j_1. Since switching activity due to these two bits is generally small, we assume that $P_s(t^i,t^j)$ is independent of the sequence of the test vectors applied and depends only on the flip flop ordering.

Switching Activity during $I_v(t^i, t^j)$: We define following expressions for the terms $R'(t_n^i, t_p^j)$ and $C(t^i, t^j)$. Expressions for the terms in (iv), (v) and (vi) can be derived similarly.

- $R'(t_n^i, t_p^j) = k \times M_{max} + (m-k) \times M_{min}$, where k = number of 1's in $t_n^i \oplus t_p^j$; and $\oplus$ is EX-OR operation (5)

- $C(t^i, t^j) = P_{i,j}$ where $P_{i,j}$ is the number of transitions in C due to application of t^j followed by t^i (6)

Let $P_v^{total}(t^i, t^j)$ denote the total power dissipation during the interval $I_v(t^i, t^j)$ then,

$$P_v^{total}(t^i, t^j) = R'(t_n^i, t_p^j) + C(t'^i, t^j) + C(t^j, t'^j) + R'(t_p^j, t_n^j) + R_s(t_p^j, t_n^j) \quad (7)$$
$$P_v^{total}(\#, t^j) = R'(\mathbf{0}, t_p^j) + C(\mathbf{0}, t^j) + C(t^j, t'^j) + R'(t_p^j, t_n^j) + R_s(t_p^j, t_n^j) \quad (8)$$
$$P_v^{total}(t^i, \#) = R'(t_n^i, \mathbf{0}) + C(t'^i, \mathbf{0}) \quad (9)$$

P_v^{max} can be similarly defined by taking the maximum of all the terms in equations (7),(8) and (9) rather than summing them. **0** in the computation of $P_v^{total}(\#, t^j)$ represents all zero vector. Note that the terms $R'(t_n^i, t_p^j)$ and $C(t'^i, t^j)$ are dependent on the order in which the test vectors t^i and t^j are applied. On the other hand, the terms $C(t^j, t'^j)$, $R'(t_p^j, t_n^j)$, $R_s(t_p^j, t_n^j)$ are dependent only on the vector t^j.

Full Integrated Scan

During Full Integrated Scan, let $I(t^i, t^j)$ denote an interval when (a) t_p^j is scanned in and t_n^i is scanned out in test register R_s; and (b) in $(m+1)^{th}$ clock cycle output of C, i.e. t_n^j, is latched to R_s. Switching activity during $I(t^i, t^j)$ consists of the following terms:

1. $P_s^{max}(t^i, t^j)$ and $P_s^{total}(t^i, t^j)$ as defined in the previous subsection.
2. switching activity in C during scan-in. As a test vector is scanned in the inputs to C change, hence power is dissipated at every clock cycle in C.
3. switching activity in R_s when output of C is latched to it in $(m+1)^{st}$ clock cycle, say $R_s(t_p^j, t_n^j)$.

Let $PI_i = \langle x_1, \ldots, x_n \rangle$ denote primary input part of the vector t^i. Let $S = \langle Y_1^i, \ldots, Y_m^i, y_1^j, \ldots, y_m^j \rangle$ as defined in the previous subsection. In the first clock cycle, inputs to C can be denoted by $PI_i.S(1:m)$. Similarly, in the m^{th} clock cycle the inputs to C can be denoted by $PI_i.S(m+1:2m)$. Using this notation $P_v^{max}(t^i, t^j)$ can be expressed as :

$$P_v^{total}(t^i, t^j) = \sum_{k=1}^{m} C(PI_i.S(i:m+i-1), PI_i.S(i+1:m+i)) \quad (10)$$

Table 1				
AND	s0	s1	r	f
s0	s0	s0	s0	s0
s1	s0	s1	r	f
r	s0	r	r	s0
f	s0	f	s0	f

Table 2						
AND	0,s1	0,s0	$N2$,h1	$N2$,h0	$N2$,hr	$N2$,hf
0,s1	0,s1	0,s0	$N2$,h1	$N2$,h0	$N2$,hr	$N2$,hf
0,s0	0,s0	0,s0	0,s0	0,s0	0,s0	0,s0
$N1$,h1	$N1$,h1	0,s0	$(N1+N2)$ h1	$\max\{N1, N2\}$ h0	$(N1+N2)$ hr	$(N1+N2)$ hf
$N1$,h0	$N1$,h0	0,s0	$\max\{N1,N2\}$ h0	$\max\{N1, N2\}$ h0	$(N1+N2\text{-}1)$ h0	$(N1+N2\text{-}1)$ h0
$N1$,hr	$N1$,hr	0,s0	$(N1+N2)$ hr	$(N1+N2\text{-}1)$ h0	$\max\{N1,N2\}$ hr	$(N1+N2)$ h0
$N1$,hf	$N1$,hf	0,s0	$(N1+N2)$ hf	$(N1+N2\text{-}1)$ h0	$(N1+N2)$ h0	$\max\{N1, N2\}$ hf

Cycle No.	R_s			R'				Power Dissip		
	F1	F2	F3	S1	S2	S3	X1	C	R'	R_s
0	0	0	0	0	0	0	0	-	-	-
1	1	0	0	0	0	0	0	0	0	10
2	0	1	0	0	0	0	0	0	0	14
3	0	0	1	0	0	0	0	0	0	14
4	0	0	1	0	0	1	1	0	10	0
5	0	0	1	1	1	1	1	3	14	0
6	1	1	1	1	1	1	1	0	0	14

Table 3: Calculation of power dissipation for $Interval\langle T_1, T_2\rangle$.

Cycle No.	R_s			R'				Power Dissip		
	F1	F2	F3	S1	S2	S3	X1	C	R'	R_s
0	1	1	1	1	1	1	1	-	-	-
1	0	1	1	1	1	1	1	0	0	10
2	0	0	1	1	1	1	1	0	0	10
3	0	0	0	1	1	1	1	0	0	10
4	0	0	0	0	0	0	0	3	18	0
5	0	0	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0	0

Table 4: Calculation of power dissipation for $Interval\langle T_2, T_1\rangle$.

Table 5						
Cycle	F1	F2	F3	X1	R_s	C
0	1	0	0	0	–	–
1	1	1	0	0	10	2
2	0	1	1	0	14	1
3	1	0	1	0	14	0
4	1	1	1	0	10	0

Table 6						
Cycle	F1	F2	F3	X1	R_s	C
0	1	1	1	0	–	–
1	0	1	1	0	10	0
2	0	0	1	0	10	0
3	1	0	0	0	14	2
4	1	0	0	0	0	0

Table 7						
Cycle	F1	F3	F2	X1	R_s	C
0	1	0	0	0	–	–
1	0	1	0	0	14	4
2	1	0	1	0	18	2
3	1	1	0	0	14	2
4	1	1	1	0	10	0

	T_i^1	T_i^2	T_i^3	T_i^4	T_i^5	T_i^6	T_i^7
a	10000	01000	01000	01000	01000	01000	01000
b	10000	10000	00100	00100	00100	00100	00100
c	01000	10000	10000	00010	10000	10000	00100
d	00100	00100	10000	10000	00010	00010	00010
e	00010	00010	00010	10000	10000	00001	00001
f	00001	00001	00001	00001	00001	10000	10000

Table 8: Input vectors corresponding to graph in Fig. 5

	T_i^1						T_i^2						T_i^3						T_i^4					
r_a	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0
r_b	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
r_c	0	0	0	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1
r_d	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0	0	0

Table 9: Input vectors corresponding to graph in Fig. 1

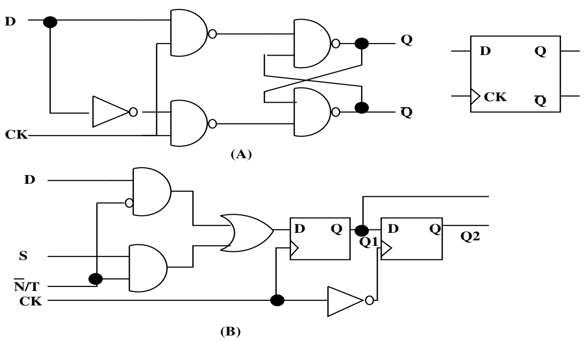

Figure 1:

circuit	initial trans	final trans	% improv	time secs
s27	625	548	12.32	1
s298	13834	12366	10.61	3
s208.1	12386	11151	9.97	3
s344	12893	11383	11.71	2
s349	14634	13460	8.02	2
s382	20522	19648	4.26	3
s386	30070	27520	8.48	12
s444	21284	19215	9.72	5
s420.1	51197	47441	7.34	14
s510	38013	32849	13.58	12
s526n	45708	39004	14.67	11
s526	43675	40107	8.17	12
s641	77200	75587	2.09	11
s713	71636	64492	9.97	10
s820	85824	68888	19.73	51
s832	89240	75447	15.46	57
s838.1	194363	188138	3.20	92
s1423	174942	160205	8.42	42
s1488	129527	103198	20.33	118
s5378	1791873	1718012	4.12	2149
s9234	3685841	3394976	7.89	7357
s9234.1	3874863	3555314	8.25	7680
s13207	8985640	8693741	3.25	15783
s15850	8422404	7994805	5.08	16397

Table 10: Full Isolated Scan Zero Delay model

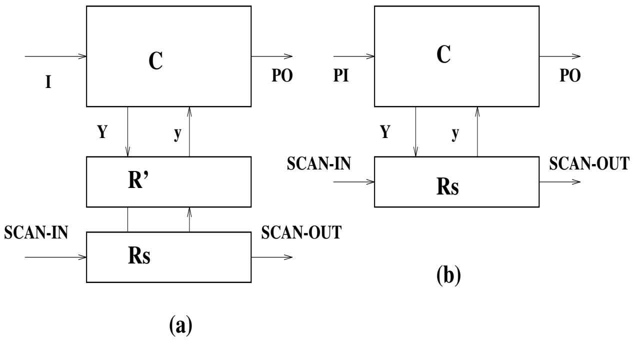

Figure 2: Scan Structures

circuit	initial trans	final trans	% improv	utime secs
s27	31	18	41.94	1
s208.1	1320	1059	19.77	5
s298	21842	19768	9.50	12
s344	7665	7069	7.78	6
s349	7815	7210	7.74	9
s382	47650	44631	6.34	27
s386	3021	2562	15.19	32
s420.1	7915	7187	9.20	145
s444	52560	49597	5.64	27
s510	789	635	19.52	38
s526	123546	119002	3.68	134
s526n	118901	112855	5.08	224
s641	48419	46006	4.98	116
s713	42141	40303	4.36	113
s820	7240	6321	12.69	191
s832	7708	6709	12.96	249
s838.1	53033	50320	5.12	2178
s1423	711864	698434	1.89	1963
s1488	28652	23896	16.60	449
s1494	29066	23874	17.86	458

Table 11: Full Isolated Scan General Delay

circuit	initial trans	final trans	% improv	utime secs
s27	49	22	55.10	2
s208.1	3219	2819	12.43	33
s298	28644	26034	9.11	73
s344	20440	18923	7.42	35
s349	20790	19088	8.19	50
s382	58667	54147	7.70	158
s386	7996	6715	16.02	209
s420.1	18497	18337	0.87	502
s444	66186	63050	4.74	156
s510	1171	969	17.25	149
s526n	149116	141603	5.04	584
s526	157415	150502	4.39	677
s641	131394	123532	5.98	552
s713	128447	118845	7.48	455
s820	10741	9040	15.84	606
s832	11429	9708	15.06	669
s1423	1469271	1439380	2.03	8409
s1488	42011	36038	14.22	1829
s1494	41974	35366	15.74	2084

Table 12: Full Integrated Scan Zero Delay Model

circuit	initial trans	final trans	% improv	utime secs
s27	31	18	41.94	0
s208.1	1320	1059	19.77	31
s298	21842	19768	9.50	70
s344	7665	7069	7.78	35
s349	7815	7210	7.74	46
s382	47650	44631	6.34	151
s386	3021	2562	15.19	186
s420.1	7915	7187	9.20	572
s444	52560	49597	5.64	151
s510	789	635	19.52	173
s526n	118901	112855	5.08	645
s526	123546	119002	3.68	750
s641	48419	46006	4.98	548
s713	42141	40303	4.36	513
s820	7240	6321	12.69	824
s832	7708	6709	12.96	921
s838.1	53033	50320	5.12	9728
s1423	711864	698434	1.89	9504
s1488	28652	23896	16.60	2225
s1494	29066	23874	17.86	2498

Table 13: Full Integrated Scan General Delay Model

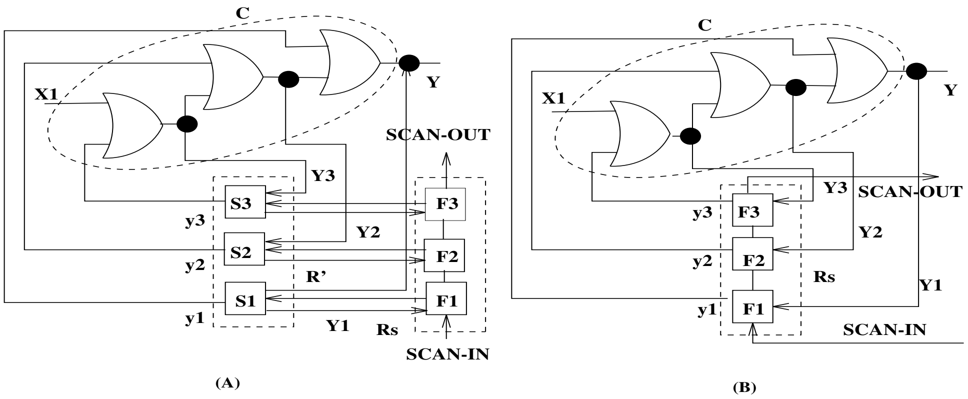

Figure 3: Examples Illustrating Factors Affecting Power Dissipation.

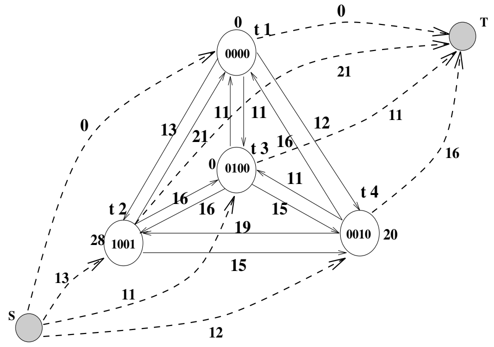

Figure 4: Total Transitions Graph for circuit in Fig 3(a)

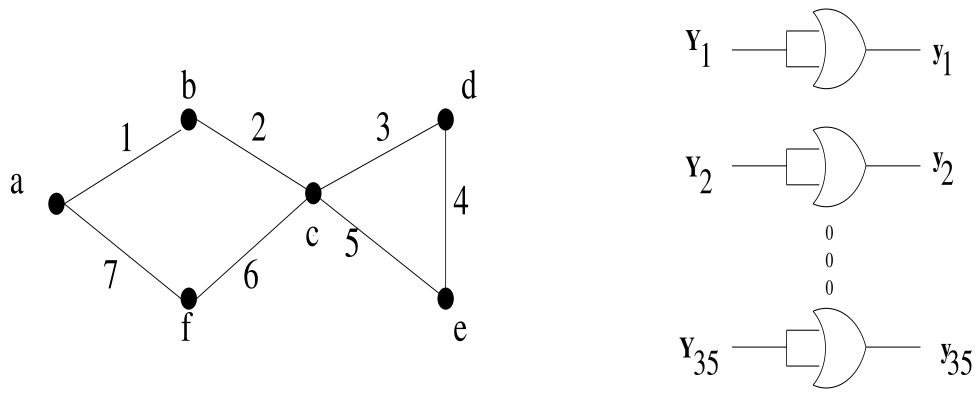

Figure 5: Example for the proof of hardness of OSP and OST

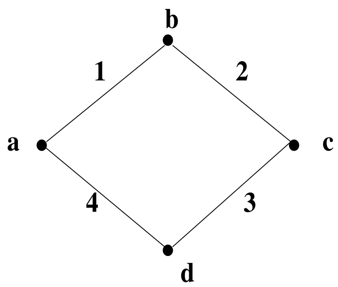

Figure 6: scan-in vectors