DESIGN FOR MANUFACTURABILITY - FAULT MODEL EXTENSIONS FOR RF CIRCUITS WITH AN ECONOMIC PERSPECTIVE FOR MANUFACTURABILITY

by

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ABSTRACT

Design For Manufacturability issues have started escalating the problem of Design and Test in the Deep Submicron era. Two questions posed are ”How good is the quality?” and ”How expensive is the product?” To ensure quality one needs to answer the question ”To DFT or Not to DFT.” New Analog and RF designs lack good DFT techniques due to inadequate fault models. Using existing test techniques that are largely outdated, one has to find out if the solutions are economically feasible for the vendor to implement in his designs. The quality issues of RF cores and the economic issues of mixed signal cores and standalone chipsets are addressed in this thesis from a DFM standpoint.

A lot of emphasis has been placed on the test cost of chips and a variety of models have been proposed in the literature. Existing models are incomplete with the fact that most do not take into account the costs involved once the chip reaches the market. This thesis focuses on the cost economics of fault tolerant chips and how RF cores fit into the whole economic model for new designs.

New fault models which could help improve the testability of circuits (hence improving quality) are discussed here. The focus is then moved to an economic cycle where mathematical estimates of the costs for new designs are given. This model will help designers analyze the need for a fault tolerant system and its feasibility in the industry using the reliability of the system. It will help evaluate the costs involved during the life cycle of a chip.

Design tools – SpectreRF and ASITIC have been used for modeling RF circuits at 0.25u technology. Carafe tool has been used to perform fault analysis on the layout of the circuit to model realistic faults. Existing fault models for resistors and capacitors have been verified and a new fault model for inductors has been proposed using these tools. The fault models will help improve the design of RF circuits by enforcing more constraints on design specific issues. The cost models proposed in this thesis will help designers identify key areas of cost and help clamp down unnecessary expenses where possible.

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Chapter 1

Introduction

1.1 Introduction

Design for Manufacturability (DFM) is the practice of designing products with the manufacturing process in mind [3]. It would help in quicker production and hence effectively reduce the one critical factor which every chip manufacturer targets - Time to Market. Also, DFM helps to ensure design reusability [4]. Since quality is ensured using a set of IP cores which are designed with DFM in mind, they can be reused again with a good deal of reliability.

DFM is the maximization of manufacturing volume achievable for the lowest possible cost. It should provide a design which maximizes a) Wafer productivity, b) Rate of yield learning [3]. Both of these can be achieved through proper quality control measures. When manufacturability has to be guaranteed by design, DFM will ensure a tight linkage between the fabrication process and the representation of that process in the design simulation environment. This requires us to understand how defects are formed and how we can model defects as faults. This brings us to the topic of defect analysis which is the basis of Inductive Fault Analysis (IFA) [5].

The 2003 International Technology Roadmap for Semiconductors [6] states that defect oriented test generation based on IFA is a very promising strategy for fault modeling to handle manufacturing imperfections. IFA offers a method by which one can grade the faults occurring in the system and use them to identify test vectors to tackle the most likely to occur faults. This would essentially ensure a very high degree of fault coverage for a minimum set of test vectors which can be tuned to identify highly probable faults. Typical measures of manufacturing excellence for a semiconductor fabricator are expressed in terms of either operational or economic results [7],[8]. Improvements in the operational results of manufacturing excellence focus upon increase in capacity and throughput, defect density reductions and cost containment while the economic results are improved through good yield and achieving Time to Market targets.

As a part of DFM modeling, test groups would face the possibility of proposing fault models for RF circuits which do not have standards available. For such groups the amount of time spent in testing new designs would be very high. The amount of effort and time spent in identifying fault models for these circuits using the IFA scheme is translated to costs through the economic models proposed in this thesis.

Cost modeling has become an essential factor in VLSI testing. One important question facing today's designers is whether to go for DFT or not. Work in this area has been done aplenty in [9],[10] where the authors have analyzed the economics of testing at the system level, design level and manufacturing level. The CMU model's [10] profit/loss expressions are universally accepted by the industry and this thesis would focus on extending this cost model to fault tolerant designs.

In this thesis, the cost of a fault tolerant chip with embedded DFT is modeled. The industry is realizing the need for fault tolerance in systems due to the increased susceptibility of designs to internal disturbances such as switching conditions and external disturbances like atmospheric radiation (soft errors) [11]. These disturbances result in a need for life-long testing of chips. The primary reasons to go for fault tolerant designs are to ensure reliability of the product for a longer duration with the customer thus ensuring his satisfaction and lowering after-sales services.

Existing cost models do not deal with the costs incurred during the lifecycle of the chip in the market. This is a major drawback since costs arising during this period (which go unaccounted for) would have to be borne by the manufacturer. This factor has been taken into consideration in the model proposed in this thesis. With the advent of SOCs, self repairable chips and rising test costs,there is a need for economic models to evaluate fault tolerant features on chip which would ensure cost effectiveness and also its success in the market. The proposed model clearly identifies system tradeoffs helping us make decisions on what features are required for a design. A major highlight of this model is its flexibility.

This model can estimate the cost of a fault tolerant design as well as that of a DFT based design without any fault tolerant features by excluding certain parameters in the model's expressions. Hence, the same model can be used in two different design environments for modeling costs.

DFM practices can hence improve design productivity, product performance and achieve time to market goals by closely coupling semiconductor fabrication knowledge with product requirements during the initial phase of a product design.

1.2 Thesis Organization

In this thesis, new fault models are proposed to improve the quality of RF circuits. The cost model for a mixed signal core design is then discussed to complement the fault model in the DFM cycle. In Chapter 2, a brief discussion on the IFA concept, the tool Carafe and how Carafe is used to model faults is presented. Chapter 3 deals with the fault modeling technique for RF circuits. Applying the IFA scheme for analog circuits has been debated in the past and this thesis will present some facts on why IFA is valid for Analog and RF circuits. Section 3.2 discusses how RLC components are modeled with faults. Inductor fault modeling is described in depth in Section 3.3. In Chapter 4, a cost model is proposed for fault tolerant designs. Section 4.1 goes into the details of the silicon cost, escape cost and the personnel cost involved in designing the chip. Section 4.2 presents a qualitative analysis of the need to keep track of the time to market factor which is followed by a discussion on "Net Present Value". In Section 4.4, the psychological issues which come into consideration due to the problems arising out of the failure of a product without fault tolerant features are discussed. In Chapter 5, the case study performed with an LNA circuit using the Carafe and Cadence tools is detailed. Section 5.2 discusses the cost model for a sample RF core. Chapter 6 concludes this thesis with a summary of the work done and a direction for future work in the area of cost modeling for testable design and fault modeling for RF circuits.

Chapter 2

Fault Modeling - A Quality Measure of Fabrication

2.1 Need For Fault Models

Faults are modeled in order to study a system's behavior when they malfunction. These models help to simulate faults that could occur in the chip during normal operation and also the defects which might arise in the fabrication process. Some of the defects [12] which are likely to arise in the chip are

- Missing contact
- Parasitic transistors
- Oxide breakdown
- Bulk defects (cracks, crystal imperfections)
- Surface impurities (ion migration)
- Dielectric breakdown

- Electromigration Processing defects

2.2 Common Fault Models

Some common fault models which are used in digital circuits are discussed in this section. These models [12] are considered industry standards for digital circuits.

- Single stuck-at faults (s-a-f)
- Transistor open and short faults
- Memory faults
- PLA faults (stuck-at, cross-point, bridging)
- Functional faults (processors)
- Delay faults (transition, path)

Single s-a-f, Transistor open and shorts are used to model the bridges and breaks which might occur due to contaminants falling on the chip. Memory faults arise due to the change in a bit value in a neighboring memory cell. Memory faults are modeled as pattern sensitive faults and are presented in detail in [13],[14]. A multiple stuck-at fault is modeled as a set of lines stuck-at some combination of (0,1) values. Statistically, single fault tests cover a large number of multiple faults. Delay faults are becoming the focus of modern process with interconnects posing a huge hurdle in terms of RLC delays and cross talk effects. The next two sections discuss how contaminants can be modeled based on their size and shape.

2.3 Point Model

Any particle or liquid droplet that deposit on the IC during the manufacturing process is referred to as a contaminant [15]. Some of these contaminants falling at some critical positions on the layout of the chip could result in defects which manifest itself during simulations as faults. These defects are called spot defects. The simplest form of contaminant model is the point model according to which, contamination affecting the ICs are assumed to be dimensionless points as shown in Fig. 2.1.

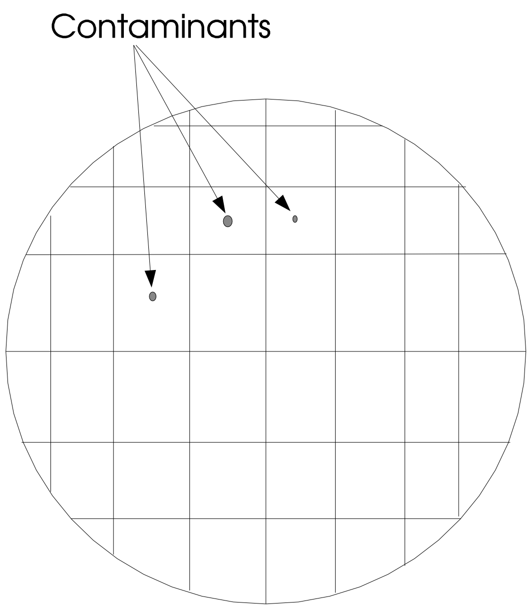

Figure 2.1: Point Contaminations on Die

There are some drawbacks in the point model. This model is adequate to model pin hole oxide defects. But as technology has progressed defect caused by lithography became more dominant. The ability of the fault models to capture such faults depended on the size of contaminants and also the nature of the layout. Point models could not bring out any particular relation between the defects and the layout of the circuit. This gave rise to the Disk model which is discussed in the next section.

2.4 Disk Model

The disk model was introduced to model the faults which could not be targeted by the point model [15]. Here the defect is assumed to be a disk of a specified radius which could be of any particular layer like, say, an insulator or poly or a metal. These extra materials could cause a bridge between two conducting layers separated by an insulator or could also cause a break in a metal line. It could also lead to the formation of parasitic transistors. It has been found that spot defects are not of the same size and not also evenly distributed throughout the entire layout. The defects do not necessarily cause faults to occur. They may fall harmlessly on areas which would not affect the working of the system. In Fig. 2.2, two material defects A and C are of the same size but only defect A causes a short. Similarly the missing material defect B and D are of the same radius but only B is able to cause an open. Thus only a part of the area is sensitive to the faults and these areas in the layout are called critical areas.

2.5 Inductive Fault Analysis

IFA is a systematic approach to generate faults that are likely to occur in an IC using technology and layout information [5],[16],[17]. IFA departs from the traditional approach of making assumptions about the faults at the logical level like s-a-f. Essentially, a higher level fault model is formulated based on

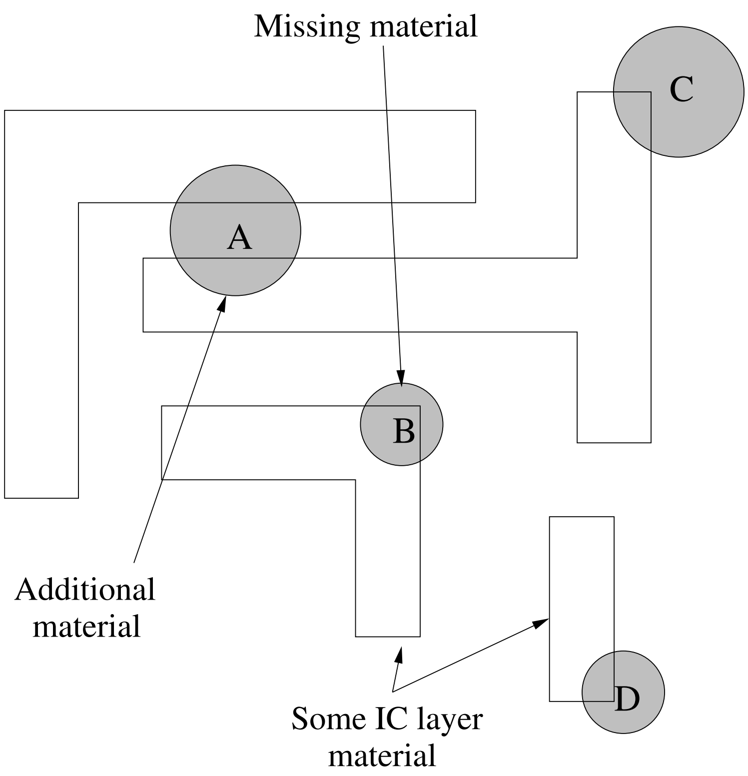

Figure 2.2: Disk model for spot defects

conclusions drawn from examining particular defects at the lower level and hence the name ”inductive”.

The first step in IFA involves the generation of defects. For this the statistical data obtained from the fab labs are used. Based on these data a decision on where to place the actual contaminants that would have occurred in the fab lines is made. The shape of these defects is assumed to be circular. The location of the faults would depend on the defect distribution on the layout. Once the defects are in place the faults can be extracted.

One first has to fix up what are called primitive fault types which are nothing but the manifestation of the physical defects. Once the primitive fault types are fixed up (the procedure for which is given in [5]) the fault list for the given defect statistics are then obtained. Mak suggested that the defect statistics which would contain the probability of a contaminant causing a bridge between two layers can be taken as one since with each new technology we would have new defects arising and it is nearly impossible to fix up such probabilities [18]. It is found in IFA that the most prominent fault type is the bridging faults. There is another concept called Inductive Contaminant Analysis [15] wherein the contaminants are modeled as three dimensional objects. Fergusson suggested that IFA is good enough for modeling the contaminants and the extra degree of complexity brought about by ICA is not required [19]. The reasons for this are that 3D contaminants can be translated into contaminants of one layer and the widespread use of Chemical Mechanical Polishing (CMP) within a Fab recipe will limit contaminants to 1 or 2 layers.

2.5.1 CARAFE

Carafe is a tool used to perform the IFA [16]. It bloats and shrinks conducting lines and finds the intersection of conductors in different planes to determine how a layout is affected by spot defects. Since the fault list is generated based on the layout of the circuit, only realistic faults are possible. The fault list given by Carafe is modeled for switch level purposes as extra transistors inserted into the extracted netlist. Carafe takes as input a set of files before giving the fault list. The first file it takes as input is the layout file. The layout should be in GDSII format or in .strm CALMA format. The layout was generated in Magic since the

GDSII format generated by Cadence tools was not compatible with the one used by Carafe. The next file required is the .tech file which is the technology file. This file would tell Carafe the various layers used in the layout, the type of contacts available and which layers could interact to form bridges. The third file required is the defect statistics file which is required to be got from the fabrication labs but the default file which came with Carafe was used due to non-availability of data for research purposes. Finally, Carafe takes these set of files as inputs and gives out the faults list. The various files which are output by Carafe are listed below. Further description of these files is given in the Carafe manual [17].

- .pro – This file contains the list of the faults ordered by relative likelihood of occurrence in descending order. This would help us fix up the final fault list.
- .sim – This file specifies the netlist for the circuit. It contains the perfectly working circuit
- .bridge.sim – This file contains the faulty circuit with all the bridges in place.
- .graph – The graph file gives a hierarchical description of a faulty circuit.

2.6 IFA – Relevance for RF Circuits

There is a lot of debate in the industry as to whether we could use IFA for RF circuits. Soma in his work [20],[21],[22],[23] has used the concept of IFA to a good degree of success to model the faults which occur in a variety of analog circuits like A/D converters, PLL's etc. The layout characteristics of RF circuits do not differ much from their analog counterparts. The difference in terms of design is the higher frequency of operation.

In [24], a detailed discussion on the validity of IFA for analog circuits is presented. IFA has been projected as one of the alternatives to analog testing. One cannot characterize the correct operation of a circuit in analog domain. We can give a range of values indicating the correctness of operation. Fixing up the tolerance limits for performance is very difficult. IFA uses the circuit topology and process defect data to arrive at realistic fault data specific to the circuit. This information can be exploited by the test professionals to generate effective and economic tests. IFA based tests are simpler and their requirements for the test infrastructure is substantially less compared to the specification based tests. Quantifying fault coverage of a given set of test vectors on an analog circuit is an unexplored area. IFA based test generation provides a methodology by which the test vectors and design can be fault graded. Once, fault coverage of different tests are known we could perform fault grading and then choose test vectors more judiciously which would help us reduce the test time. One of the disadvantages for IFA based test is that it is limited by the availability of CAD tools. Carafe cannot handle circuits of huge complexity like microprocessors and we would have to partition the circuit and feed it to the tool. Based on the above reasoning one can conclude that IFA based scheme is a very good approach to perform fault modeling for RF circuits. Inorder to come to this conclusion it is required by the test engineers to decide on the nature of the circuits he is going to handle and the type of faults they would be tackling. This would take some time to study and would translate into cost spent on the personnel involved which is included in the cost equation presented later in the thesis.

Chapter 3

Fault Model Extensions for RF Circuits

3.1 Methodology Overview

Realistic fault models are obtained by implementing Inductive Fault Analysis using Carafe. One of the files required by Carafe is the defect statistics file. The default statistics file that comes with Carafe could be used for this purpose in the absence of an up-to-date fab file. This file contains the defects which are likely to occur among various semiconductor layers with a uniform probability. Defects of various suitable sizes are input into the statistics file. An experimental procedure to develop fault models for a variety of analog circuits like ADCs and Sample and Hold circuits is given in [20],[21]. In these works only realistic faults which are most likely to occur in the manufacturing phase have been analyzed. The IFA technique has been used in identifying fault models for Cache RAMs [25], clock distribution faults [26], multi-node bridge analysis for a variety of layouts [27] and also for analog faults [22]. Inductors are commonly found in most RF circuits. Tthe ASITIC tool [28] will be used to design spiral inductors for the various RF systems.

Once the fault list is obtained, a circuit simulation using Cadence SpectreRF [29] with the faults in place is performed. The functional simulation will be able to confirm if the faults inserted are sensitized by looking at the performance of the circuit. For this, the S-Parameters, voltage gain and the noise margin of the circuit will be studied. If the fault does not affect the circuit performance then it can be removed from the fault list. The simulations are performed under the assumption that a maximum shift of 10% in the parameters can be tolerated. This is the limit up to which the circuit is said to function correctly. Beyond this range it is assumed that the circuit has failed.

3.2 Fault Models for Passive Components (R, L and C)

The procedure to model the faults is based on the experimental approach of Soma [23],[20]. The validity of these models for high frequency circuits is verified. In addition to the work in [23],[20] a new fault model for an inductor is proposed.

3.2.1 Faulty Resistor

Faulty resistors arise because of additional material falling on the already laid out component. This is modeled in Cadence as shown in Fig. 3.1 to see how the resistor behaves by placing additional material at various locations on the serpentine resistor. This is performed to determine the range of values the resistors of the LNA circuit could take when they go faulty and if it affects the working of the

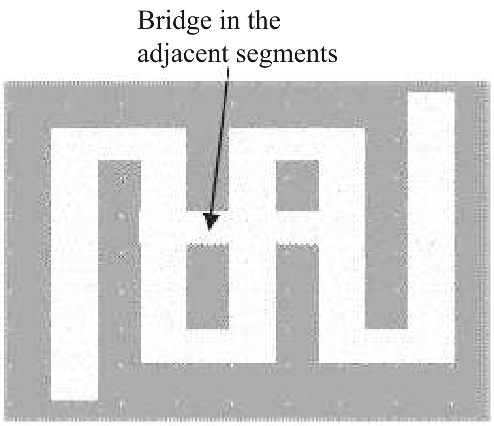

Figure 3.1: Faulty Resistor Layout

LNA to a great extent. The faulty resistor can be modeled as a perfectly working resistor in series with a faulty resistor whose value can be varied from zero to a desired level [23],[20].

3.2.2 Faulty Capacitor

Soma's approach [23],[20] to model a faulty capacitor is followed here. A resistor is added in parallel with the capacitor to model its faulty behavior. The resistor value is varied from zero to a very high value to see how the circuit behaves.

3.2.3 Faulty Inductor

The inductor is laid out using the ASITIC tool [28],[30]. This tool is used to model bridge faults occurring in the inductor. Defects of varying sizes are placed on different locations of the inductor to cause a bridge. The defect contributes to an increase in inductance. The defect placement can be seen in Figures 3.2 and 3.3 as a sample of what was simulated in ASITIC. This is translated into a fault model for the inductor as a perfectly working inductor in series with a faulty inductor.

3.3 Inductor Fault Modeling using ASITIC

This is part of the work presented in [31]. Modeling the faults in the inductor is of special interest since this work has not been done before. The large inductors have a higher probability of being affected by a defect. These defects are substantial enough to cause a change in the inductance values and can cause variations in the parameters of the RF subsystems. The model has been tested with square spiral inductors.

Once the inductor is laid out in ASITIC, the wire and join commands are used to add a piece of material which would act as the defect (forming a bridge) along the various segments. The current flow in the defect will be in the same direction as that of the materials which are bridged. Bridging between opposite segments (having current flows in the opposite direction) is very less likely to occur because of the large size of the defect that will be required to cause such a bridge.

Single and multiple defects are placed on the layout of the inductor and its behavior is studied. Inductors are laid out with higher layer metals. Defect analysis with M6 and M2 layers was performed. Both these layers resulted in identical behavior when subjected to defects. Hence the deviation in performance can be attributed only to the defect and not to the layer in which the inductor is laid out.

Hollow inductors were used in the design. If a defect falls over this hollow area as shown in Fig. 3.2, it results in a drop in the quality factor of the inductor and also affects the inductance value. Here the quality factor is found to drop by more than 12% as against the previous case (Fig.3.3) wherein the drop is in the range of 4-5%.

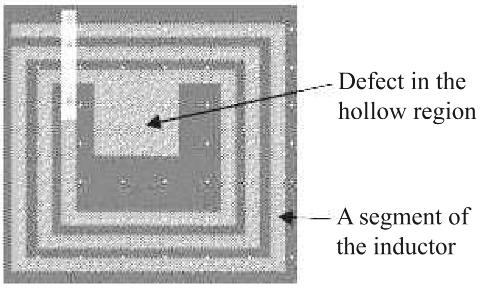

Figure 3.2: Defect in the hollow region

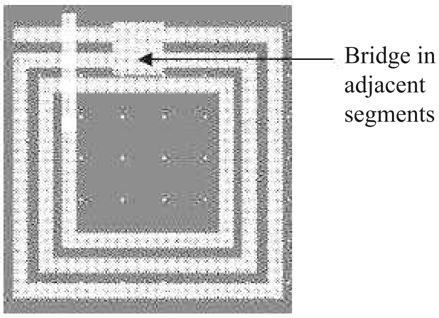

Figure 3.3: Defect in the adjacent segments

The fault models proposed in this section are used in a LNA circuit to model various defects which are simulated in Carafe. This is part of the case study presented in Chapter 6. The cost issues arising from the time taken by the test engineer in modeling these faults is discussed in the next chapter.

Chapter 4

Need for Cost Economics

Testing ensures that the quality of the devices are maintained high and they don't fail during on-field operations. One needs to ensure that the cost of testing does not rise very high in order to reap maximum profits from a given product. For this one has to relax some factors which might in turn affect the quality. What these factors are can be studied through cost modeling which provides an in depth study of the various cycles a chip would have to go through before reaching the consumer. There are several types of cost to be studied [12]. They are

- Fixed Cost (FC) – These are costs which do not change with use of a product. For example the cost of machinery involved is not going to change once the products to be manufactured are decided.
- Variable Cost(VC) – These are costs which increase with the production output. For example Labor, energy and raw material.
- Total Cost (TC) – This is the sum of the fixed and variable cost.
- Average Cost(AC) – This is obtained by dividing the total cost by the number

of units produced.

4.1 Economics of Testing

Intel [12] reports that the combination of verification, testing and manufacturing is the biggest hurdle it faces than the cost of silicon in designing new chips. It is slowly emerging that instead of using ATE (Automatic Test Equipment) for testing the chip entirely, one could achieve a good percentage of cost reduction by going for DFT schemes like BIST or scan. This decision has its own repercussions. Adding extra hardware to the design which was painstakingly optimized by the designers for speed and power will have a negative impact on the performance of the device. But on the bright side, with technology constantly improving as per Moore's prediction we are able to pack more devices into the chip, increase their functionality and there by also reduce the cost of design. But increasing the functional density would result in additional burden on the test engineer to ensure more devices work properly. This is where BIST can help us. Though tests can be run at the rated speed of the device by using BIST, the additional circuitry involved is going to increase the cost of the chip. Unless the cost arising out of BIST can be offset elsewhere in the life cycle of the chip it is not advisable to go for such a process. The law of Diminishing returns [12] aids us in deciding the limit for the production cycle of the chip. The law states

> *If one input of production is increased keeping other inputs constant, then the output may increase, eventually reaching a point beyond which increasing the input will cause progressively less increase in output.*

In the next section, the various parameters from a testing point of view which are required to be studied are discussed in detail.

4.2 CMU Model - A DFT Based Model

Nag et al. [10] have proposed a cost model denoted here as the CMU model, in which the cost of testing is divided into various factors. The cost of testing is given as

$$C_{test} = C_{prep} + C_{exec} + C_{silicon} + C_{quality} \tag{4.1}$$

C_{prep} takes into account the fixed cost like test vector generation and test program creation. C_{exec} included the tester hardware cost such as probe cost and cost incurred by ATE which would include the setup cost, execution cost and capital cost of the tester. $C_{silicon}$ is the cost required to incorporate the DFT onto the silicon. This is essentially dependant on the area of the device. Finally $C_{quality}$ is a factor which includes the escape cost of the silicon and takes the fault coverage of the system into account. All the cost involved are calculated per yield.

4.2.1 Test Preparation Cost

The test preparation cost is given by the equation

$$C_{prep} = (C_{test\_gen} + C_{test\_prog} + C_{DFT\_design})/Y \tag{4.2}$$

C_{test_gen} is the cost involved in the test pattern generation for the given device. This cost is proportional to the product of the time for generating the test vectors and the personnel cost involved in the generating the test vectors.

C_{test_prog} is assumed to be proportional to the test generation time since it depends on the time taken for programming the test vectors to be fed into the ATE in a timely manner.

C_{DFT_design} is the additional DFT cost which will be discussed later. Finally Y is the yield of the fabrication process.

4.2.2 Test Execution Cost

The test execution cost is given as

$$C_{test\_exec} = C_{hw} + C_{tester} \tag{4.3}$$

The C_{hw} is the hardware cost involved in replacing the probes which would be used to capture the responses from the board. These probes deteriorate with use and hence require replacement. This is a function of the number of IC's we probe. The C_{tester} constitutes the cost involved when the tester is active and when it is inactive. The tester when active will feed in the test vectors into the chip and analyze its responses. The inactive time would constitute the time involved while replacing chips on the tester and changing the test generation programs. The tester cost would depend on the number of devices to be tested on chip. This is where BIST comes into help as we could use self-testing features to advantage and leave the tester to test areas of the chip which are not supported by BIST. Thus the cost of bringing in BIST would be offset by the savings in reduced tester time.

4.2.3 Silicon Cost

The cost of silicon is going to involve the amount of area of the design involved along with the amount of redundant hardware which would be added into the chip due to DFT. The work of [32] involves modeling the silicon cost as cost involved in designing the logic and the memory block. This is because one can differentiate BIST as logic BIST and memory BIST and this helps us model the cost arising from these two blocks separately.

4.2.4 Quality Factor

A very important factor which is not often taken into consideration is the cost due to imperfect test quality. This factor is a very crucial component in cost modeling for fault tolerant designs. Now the cost arising from this is classified into three parts. They are

- Performance Loss – This cost arises out of the performance loss due to additional hardware included into the circuitry. If the DFT fails to identify the faults occuring in the circuit then it simply serves as redundant hardware with no purpose.

- Yield Loss – This cost arises out of the fact that one models a good chip as faulty due to the inclusion of bad test vectors into the system and performing incorrect response analysis. With analog testing there is no fixed correct response as in digital. We have to include certain tolerance limits to the design being tested. If the tolerance is too conservative then a good chip could be rejected.

- Escape Cost – As discussed above if one keeps the tolerance values too liberal then he is likely to let a bad chip pass for a good one. In the digital world, we cannot definitely target 100% fault coverage. Hence the chance of letting a bad chip slip by is high. This could result in incorrect operation of the chip at the consumer end and the vendor will have to face the repercussions of letting the bad chip slip by.

The CMU model included the DFT cost into their model by bringing in parameters called α factors. Further details on these factors can be found in [10].

4.3 Cost Model for BIST

In [9], a model to define the cost of BIST in a design is proposed. The author lists out the benefits of BIST based systems and how expensive these benefits are likely to be. Some of the benefits are better test access, improved design verification, shorter time to market and less dependence on the ATE. The extra cost arises from the design and implementation of the BIST scheme, area overhead and BIST induced failures. Quantifying these benefits and subtracting the costs from the benefits would give us a better perspective of whether we should go for BIST from a profit/loss viewpoint.

4.4 Time to Market

This factor did not figure in the CMU model explicitly. In [33], it is given that a 6 month delay in the product reaching the market would result in a 33% profit loss. This is highly critical. The product reaching the market quickly for a vendor is a fight for supremacy in that particular product group. It is a common knowledge that once a manufacturer's product arrives early in the market, he gets complete control of that product range - the iPod being a very good example to justify this point. He will be able to pump in more money to R&D and rectify the mistakes made in the first product launch. There are two models which will help us to estimate the life of a chip. The first one is the Simplified Triangular time to market model [1],[34] and the other is Growth-Stagnation-Decline (GSD) time to market model[2].

4.4.1 Simplified Triangular Time to Market Model

The simplified triangular model [1],[34] was developed by Logic Automation. The loss in revenues due to delayed entry into the market is given in Fig 4.1.

This model assumes that the area under the triangle represents the maximum revenue obtainable by the product over a period of time. The model also assumes that the peak in revenues of the product in the market, in-spite of the delayed entry, would be at the same time as that of the on-time entry. The loss in revenue is shown by the shaded region is given by

$$LostRevenue = R_0 * D * (3 * W - D)/((2 * W^2) \tag{4.4}$$

Where D – Delay in months over delivering the product to market, 2W – Length of the product life cycle, R_0 – Expected product revenue if it were on time to the market.

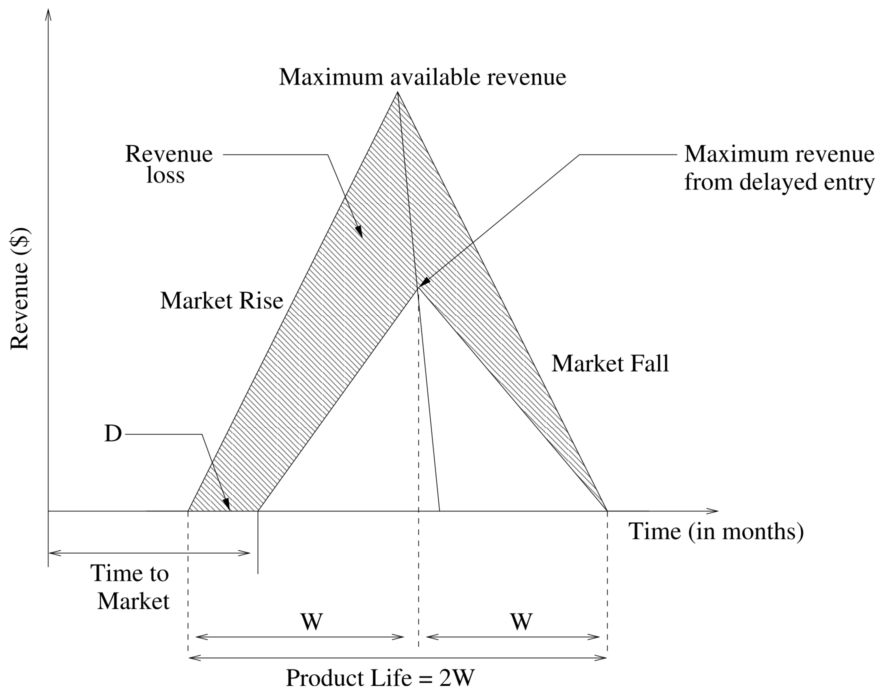

Figure 4.1: Simplified Triangular Time to Market (1)

4.4.2 Growth-Stagnation-Decline (GSD) Model

In this model the product life cycle is divided into three stages as shown in Fig. 4.2. Once the product gets into the market it will see growth through sales of the product. This is the first stage. After a period of time the sales will saturate and there will be a stage when the revenue increase freezes. This is the second stage. As soon as new technologies bring out better equipped products into the market there will be a decline in the sales of the older versions. This is the last stage. The shaded area will represent the loss due to a delayed entry into the market.

The revenue loss in this model is given as

$$R_L = R_0 * D * (2 * W_1 - D + 2S + W_2)/(W_1 * (W_1 + W_2 + 2S)) \tag{4.5}$$

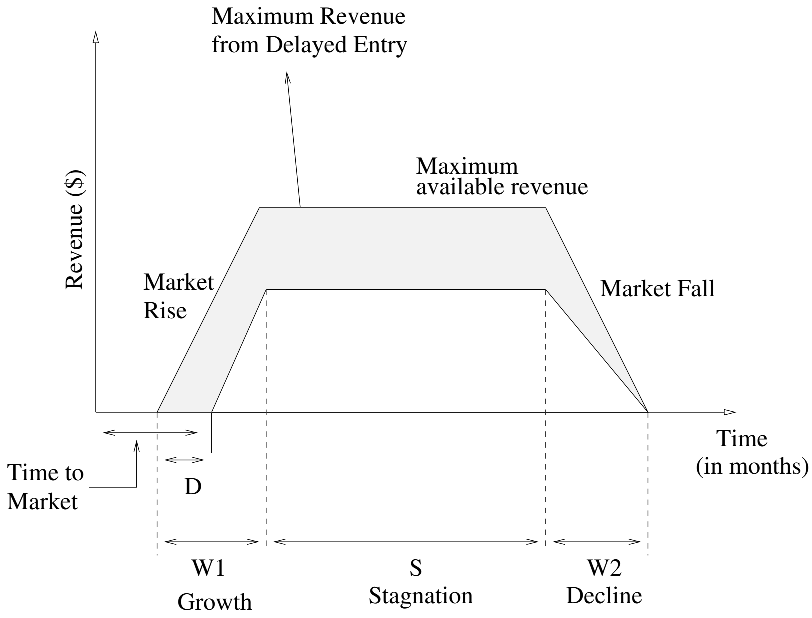

Figure 4.2: GSD Model (2)

Where W1 is the market growth window, W2 is the market declining window, S is the stagnation period.

4.5 Miscellaneous Factors

The Test fixture is a factor which depends on the number of I/O pins. The fixture complexity is affected by the technology and target pin size. Test development is found to take only 1/590th the time it would take without BIST [32]. Also the test program debugging and verification is also reduced by the same fraction which was studied in [32]. Now BIST has reduced the overall ATE cost. The test program length has been decreased by the 1/590 factor. But the test equipment price increases with increasing pin count, operating frequency and memory size. Now all these factors would get reduced with the inclusion of BIST. Beyond the manufacturing stage BIST would help in identifying on-field problems with the help of techniques like scan chain insertion. Thus personnel cost for service engineers would come down since one can target the faults at a much quicker rate and isolate the problem. Also one needs to see the downtime of the chip when it has failed on-site. These factors would result in a loss to the consumer which would reflect back to the manufacturer.

4.5.1 Higher Fault Coverage

Assuring a higher fault coverage essentially helps in improving the yield of the chip. If the yield increases then the losses are reduced and also quality of the product is raised. Now a vendor delivering faulty units would charge for them but he would also incur a penalty cost of having to replace the faulty unit free of cost and also incur customer dissatisfaction.

4.5.2 Operator Involvement

The test process consistency is also a factor to be considered in test cost. In Ambler's work [35], they have described a case where identical products which were tested in different locations can have a marked difference in test results. They had come up with mathematical expressions to account for the test operator involvement. Essentially this factor depends on the training and experience of the test operator. The expression they had come up with is

$$B_{TO} = [\alpha_{to} * T_l(T_{td} + T_{vd})] - [\alpha_{to} * T_l * 1/590(T_{td} + T_{vd})] \tag{4.6}$$

where B_{TO} – Benefit of BIST to the test operator

α_{to} – Test operator involvement

T_l – Test length

T_{td} – Test development time

T_{vd} – Debugging time

The need for fault tolerant designs have made the above models insufficient since none of them take into account the redundancy in the designs. A new cost model for fault tolerant designs has been proposed in the next chapter which models various factors such as reliability, redundancy and their influence on cost.

Chapter 5

Cost Model for a Fault Tolerant System

5.1 Basic Model

In this section, an overview of the cost model is presented. This work has been published in [36]. When fault tolerance is adapted in designs, the increase in cost due to the overhead of redundant hardware is compensated by the savings obtained in field operations. This is achieved due to increased reliability of the system. The following equation characterizes this fact.

$$C_{excess} = C + \alpha N_{FT} P - (M N_{NFT} + T') \tag{5.1}$$

where C_{excess} – Excess cost imposed on a system with fault tolerance, C – Cost of the units with fault tolerant feature, α – Probability of Failure, N_{FT} – Number of units with Fault Tolerant feature, N_{NFT} – Number of units with no Fault Tolerant feature (N_{FT}=N_{NFT}), P – Manufacturing Cost of a chip with fault tolerant features, M – Cost of a chip without any fault tolerant feature, T' – On field replacement cost for chips without fault tolerance.

The excess cost can be positive or negative depending on certain parameters which will be described now. The first term in the above expression is the manufacturing cost of the chip which includes the design cost, test cost etc. The second term in Eq. (5.1) is the most significant one. Not all the chips with fault tolerance need to work successfully during the period of operation. This term would give the cost of those chips which failed on-site in spite of being fault tolerant, resulting in the replacement of the chip. The third parameter has the cost of the chip without fault tolerance along with the on-field testing cost, when the chip fails on-site.

A positive value for C_{excess} tells the designer that he might have to change the fault tolerant architecture design or go for a design with no fault tolerance in it. This would help the designer evaluate different fault tolerant architectures on a cost basis. When C_{excess} is negative then the designer is ensured of a cost effective system with a good reliability to survive in the field.

α is modeled along the lines of system reliability (R) as $\alpha = 1 - R$ [37]. This parameter would give us the probability of survival of a system on field. The parameter is dependant on the architecture used to achieve fault tolerance. Higher the reliability of the system the lower would be the cost of replacing any parts on field and hence lower on-field activity by the personnel. But this would also result in an increase in the manufacturing cost through an increase in area of redundant parts and other factors.

The cost of a chip with fault tolerant features is modeled in the following sections. This will include the cost arising out of silicon area, personnel cost and escape cost as given in [10]. The tester cost is already modeled in [10].

5.1.1 Cost Due to Increase in Chip Area

It is shown in [38] that yield decreases strongly with chip area which results in the increase in silicon cost as a function of area. The model in [10] is adopted here and modified to include the area increase brought about by the extra hardware due to fault tolerance apart from the area consumed by the DFT and the chip design.

$$C_{silicon} = Q_{wafer} * (A_{redundant} + A_{test} + A_{chip}) / (\Pi R_w^2 \beta_{wafer\_die}) \tag{5.2}$$

where $C_{silicon}$ – Cost due to silicon, Q_{wafer} – Cost of the wafer, $A_{redundant}$ – Area to be redundant on the chip, A_{test} – Area increase due to DFT features, A_{chip} – Area of the basic chip design, R_w – Radius of the wafer, β_{wafer_die} – Percentage utilization of the dies from the wafer ignoring those which get formed around the circumference of the wafer.

The yield (Y) is modeled based on Seed's equation [39] given as $Y = (1 + AD)^{-1}$ where D is the defect density and A the area of the chip.

The area parameter modeled in the above equation is given as

$$(A_{redundant} + A_{test} + A_{chip}) \text{ as } A_{logic} + A_{memory}$$

where

$$A_{logic} = (1 + \gamma_{r\_area})A \tag{5.3}$$

$$A_{memory} = A(1 + (\log_2(m_{size}) * 1.33)/m_{size}) \tag{5.4}$$

where γ_{r_area} – Area overhead of DFT and redundancy, m_{size} – Memory capacity. This model was taken from [32]. The increase in area results in increased logic in the circuit. This increases the time spent on the ATE which is also modeled in [10].

5.1.2 Test Escape Cost

The second term in Eq. (5.1) contributes to what is called escape costs which is examined in detail in this section. The escape test cost arises from the fact that we are not able to achieve 100% fault coverage and in our case 100% reliability. The escape rate is given in [40] as

$$E_r = (1 - Y)^{(1-f)} \tag{5.5}$$

where f is the fault coverage. The escape cost which results due to bad fault coverage for a fault tolerant system is given as

$$C_{escape} = \alpha N_{FT} P + P E_r \alpha_{escape} N_{FT} - R P N_{FT} \tag{5.6}$$

where α_{escape} is given as the factor representing the risk incurred in accepting a defective IC, P is the manufacturing cost of one chip. The first parameter is the second term in Eq. (5.1) while the other two terms are covered in the C parameter of Eq. (5.1). The second term above refers to the escape cost arising due to the test coverage [10]. The third parameter refers to the cost reduction by reconfiguring around those parts which failed during testing with the spares. The net effect of the above equation takes into consideration the escape cost arising from the failure of fault tolerance.

5.1.3 Increase in Personnel Cost

The cost increase in personnel is essentially due to the extra effort placed in design and test. One must take care of essential parameters like area and power while designing such circuitry. The cost arising from this is given as

$$C_{personnel} = N_{wh} * N_{wp} * C_D \tag{5.7}$$

where

N_{wh}=Time for Design+Test, N_{wp}=Number of people working on the design and C_D is the personnel cost per unit time.

However, one should not forget that the excess cost, which arises here due to increase in man hours, will be compensated later once the product reaches the market due to its longer life without service time. Due to the additional features, the chip will have a higher probability of survival without any form of error or human intervention. This will lead to cost reduction of field engineers who might need to replace parts if the chip fails.

This is included in the following equation

$$C_{per\_sav} = R * N_{FT} * P_{personnel} \tag{5.8}$$

where $P_{personnel}$ – Personnel Cost in fixing in-field problems. However, there is a personnel cost arising from fixing the units which have failed due to the poor reliability of the system in spite of fault tolerance being added to it. This cost is added to the cost of the good units and is given as

$$C_{per\_loss} = \alpha * N_{FT} * P_{personnel} \tag{5.9}$$

The effective spending by the company due to added features is given below.

$$C_{effective} = C_{personnel} - C_{per\_sav} + C_{per\_loss} \tag{5.10}$$

where $C_{effective}$ is the net expense incurred in terms of personnel cost. Cost models in general do not take into account the C_{per_sav} factor while deciding the costs. This model relies on how long the chip will operate with the customer without defaulting and hence the use of this parameter in the cost expression was required.

5.2 Time to Market

The factor which would increase the time to market is the increase in time for design and test due to added components. The key to reducing this increase would be to reduce the development and test time. It is estimated that a 6 month delay in releasing the product to the market would lead to a 33% profit loss [33]. The more time is spent by the designers with the product in the labs, the greater would be the loss in revenue. The semiconductor industry is still governed by Moore's law and as technology changes, the products have to be redesigned for the new one. Mismatch between the new technology and the older design would result in the chip going back to the design house for revamp and hence further delay in reaching the market [11].

Where does fault tolerance come into picture? It is important for the designer to understand the need to keep adding new features to the chip. He would have to ensure that consumer needs are met and also stave off competition by getting to the market first. Now fault tolerance along with DFT would come to help in testing issues. One could reduce the time spent with the tester through DFT. By improving the fault tolerance of the chip through redundancy, one could easily reconfigure the spare when a fault is found in the manufacturing phase or in the field. Fault tolerance would help us to ensure that one can meet the required supply of perfectly working chips. Say it takes n months to design and fabricate a chip. Now when errors are found, one will have to spend some extra time in fabricating new chips to replace those that failed in order to keep the production volume constant. This would in essence delay the arrival of the chips to the market and also increase the manufacturing cost due to the addition of extra chips which is covered in Eq. (5.1). Implementing fault tolerance would thus help us to significantly reduce the above factors which delays the time to market.

5.3 Net Present Value

A factor which contributes to the loss in revenue due to a delayed entry into the market is called the Net Present Value (NPV) [41]. NPV compares the value of a currency today versus the value of that same currency in the future, after taking inflation and return into account. If the NPV of a prospective project is positive, then it should be accepted. However, if it is negative, then the project probably should be rejected because cash flows are negative. Now it is a common economic sense that the value of money today is not going to be the same in 6 months or a year from now. If one is going to spend x dollars in R&D, design, test and fab as per estimate of releasing it on day Y to meet the on-time to market, but due to certain delays are forced to release it 6 months later, then it essentially shows that the value of the money spent and the amount which could have been recovered by early release due to a possibly higher value of the currency would be stupendous especially if the volume is large. This is covered in Eq. (5.1) implicitly.

5.4 Psychological Issues

Eq (5.1) is proposed on the assumption that the customer, if faced with a problem, would come back to the same vendor that sold him the product. If he/she encounters a problem during the warranty period, then he/she is most likely to do so. But the failure of the product to meet its desired life by the customer would result in customer dissatisfaction which can result in a loss of customer base. The warranty period of the product would have to be chosen wisely for this nature of problems that should satisfy both the customer as well as the producer.

Once the chip does fail after the warranty period, the company need not to worry about servicing the chip at any added cost to the economic model of the chip since this would be an extraneous event to the life of the chip as far as the cost goes. But the psychological factor to be dealt with here would prove quite expensive. If the customer is not satisfied with the working of the product during its actual life cycle then the chances of him/her changing vendors is quite high. This would result in a loss of business for the vendor. Another factor one needs to be worried about is Moore's Law. If the vendor is not updated with the latest technologies and goes obsolete, then there is no place for him/her in the market and there is no way he/she can attract customers. A factor not considered in cost models is the amount of engineering effort going into a design.

Though the personnel cost does take into account the duration of work hours spent by a designer for a product, it does not take into account the actual effort (in psychological terms) put in by a designer. Designers would definitely not opt for complex designs which would require a lot of effort to be put in, unless the expected results are really high.

Chapter 6

Case Study

6.1 Fault Model Results

The single-ended Low Noise Amplifier (LNA) [42] is laid out in 0.25u technology. The schematic of the circuit is shown in Fig 6.1. The fault list for this circuit is obtained by running Carafe over the layout of the LNA. The graded fault list obtained shows a high probability of occurrence for faults on the resistors, capacitors and inductors. This is attributed to the fact that these are the devices which occupy the largest area in the layout of the circuit. Also a gate source bridge in transistor B is found likely to occur with the statistics that was fed in. Based on the fault list obtained from Carafe, the fault models discussed in Chapter 3 are used to perform a specification based fault analysis on the LNA.

A schematic based simulation is run on the LNA taking each one of the faults identified in Carafe individually. In Tables 6.1-6.5 below the results of the S-parameters, Noise Figure (NF) and Voltage Gain (VG) with the faulty devices are presented.

Inductance nH	S11 (db)	S21 (db)	S12 (db)	Voltage Gain (db)	NF (db)
7	-17.79	-34.31	10.64	13.14	0.824
17	-18.2	-35.42	***9.57***	***11.85***	0.824
25	-18.32	-35.83	***9.118***	***11.00***	0.824

Table 6.1: Parameter variation when inductor L_d (7nH) is faulty.

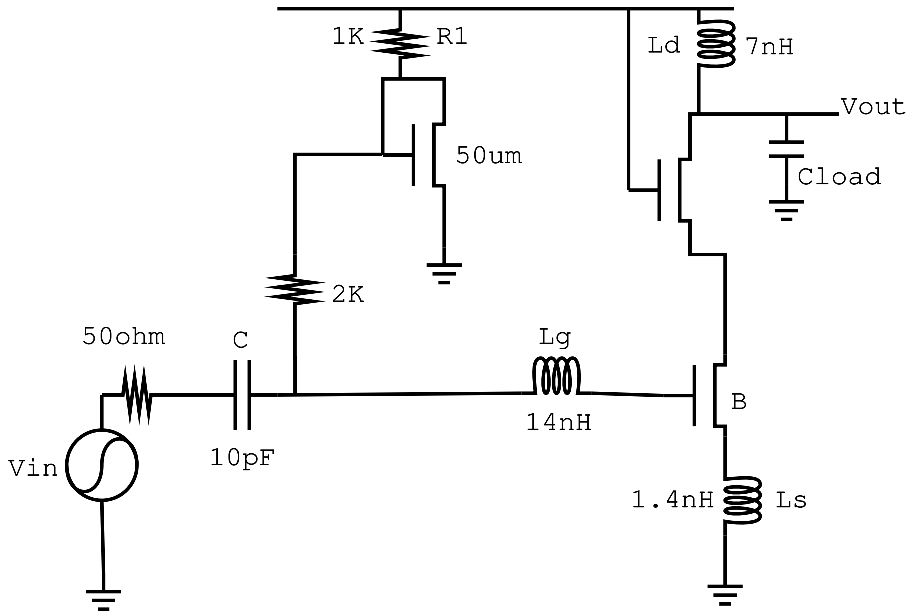

Figure 6.1: Single Ended LNA schematic

Ls is modeled with one defect to obtain a 1.48nH variation. The location of the defect placed is shown in Fig 6.2. When Lg was first modeled with one defect, a value of 14.23nH was obtained. Two separate defects were then placed in ASITIC to obtain 14.6nH. For simulation purposes the mean of the two values was taken. The defect locations for obtaining 14.6nH and 14.23nH is shown in Fig. 6.2 and 6.3 respectively. It is verified that such a variation in the inductance is possible through defects of marginal sizes. Tables 6.1,6.2 and 6.3 confirm that faults in the inductor can result in failure of the system. Ls and Lg which were designed for input impedance match and maximum power transfer show degradation in the value through S11 and voltage gain. Ld was designed for output match and shows a degradation in S21 and voltage gain when it reaches 17nH. The fault list from Carafe did not name Ld as a faulty inductor, but it was assumed to be faulty in order to study how the empirical results varied from the other inductor.

Inductance (nH)	S11 (db)	S21 (db)	S12 (db)	Voltage Gain (db)	NF (db)
1.4	-17.79	-34.31	10.64	13.14	0.824
1.48	***-19.56***	-34.53	10.48	12.81	0.829
1.99	***-24.1***	-35.22	***9.53***	***11.43***	0.871

Table 6.2: Parameter variation when inductor L_s (1.4nH) is faulty.

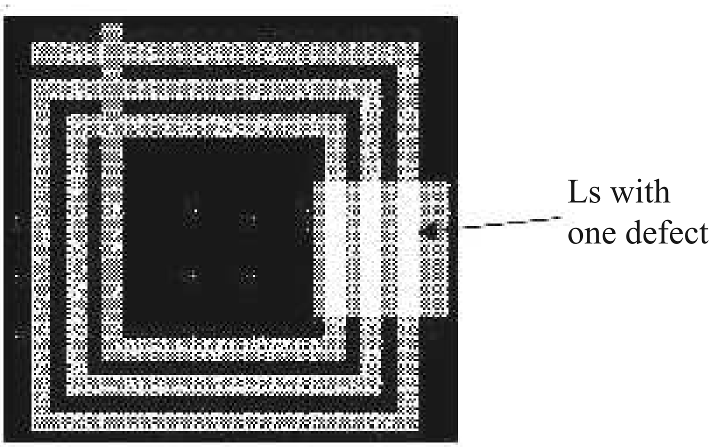

Figure 6.2: Ls with one defect to yield 1.48nH

Parameters with more than 10% variation are shown in bold italics. Also the values of the faulty components (RLC) which cause such a shift in the parameters are indicated in the first column. The second row indicates the perfectly working circuit parameters in all the tables.

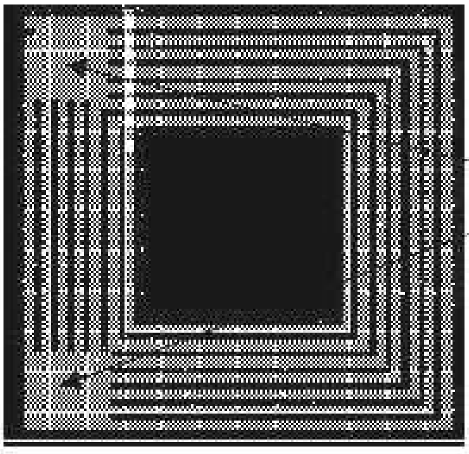

Figure 6.3: Lg with two defects to yield 14.6nH

Inductance (nH)	S11 (db)	S21 (db)	S12 (db)	Voltage Gain (db)	NF (db)
14	-17.79	-34.31	10.64	13.14	0.824
14.4	***-16.36***	-34.35	10.6	11.47	0.831
16	***-11.3***	-34.64	10.32	***7.248***	0.899

Table 6.3: Parameter variation when inductor L_g (14nH) is faulty.

Even an 6% variation in Ls from 1.4nH to 1.48nH confirms that the system drifts from its normal behavior. A single defect is sufficient to cause an 8% variation in inductance value and two defects cause a variation of up to 20%. There can be times when the designer tries to relax the 10% limit on certain parameters (say S11 in Table 6.2), but on doing so there might be other parameters (S21 and VG in Table 6.2) which would cross the justified limits when Ls exceeds 1.5nH. Hence the tolerance limits for this inductor must be kept within 1.5nH in order to ensure that the performance of the circuit does not totally degrade. The setting up of tolerance limits for the above devices should be done after carefully studying their behavior based on the fault models proposed.

In Table 6.4, the results of simulation of the faulty resistor R1 are shown.

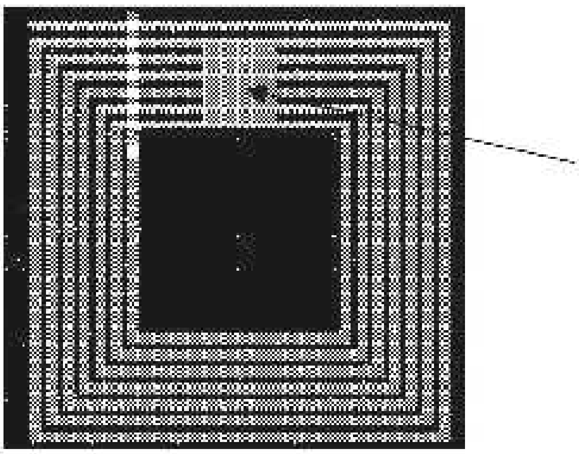

Figure 6.4: Lg with one defect to yield 14.23nH

Resistance Ω	S11 (db)	S21 (db)	S12 (db)	Voltage Gain (db)	NF (db)
1	-17.79	-34.31	10.64	13.14	0.824
1.6K	***-15.76***	-33.44	9.78	13.19	***0.942***
1.8K	***-15.28***	-33.18	***9.50***	13.17	***0.930***

Table 6.4: Parameter variation when resistor $R1$ (1Kohm) is faulty.

Through Cadence SpectreRF, it is verified that it is possible to achieve such faulty values. Bridges are introduced in various parts of the serpentine resistor as shown in Fig. 3.1. It can be seen that for a faulty resistor of 1.6K the noise figure is the first parameter to get hit along with S11. Going further higher to 1.8K, S21 also deteriorated. The faulty resistor is achieved by bridging two/three adjacent segments which is very likely to happen. The term NR in Tables 6.5 and 6.6 indicate that no faulty resistor is included with the capacitor/transistor to simulate a good circuit.

For the DC blocking capacitor C a faulty resistor Rc is added in parallel to it as in the lines of the fault model proposed for the faulty capacitor [6]. The resistor values are decreased from a very high value (to simulate an open) to

R_c	S11 dB	S12 dB	S21 dB	V G dB	NF dB
NR	-17.79	-34.31	10.64	13.14	0.824
5K	***-13.17***	-34.19	10.26	12.90	***1.672***
100 Ω	***-4.126***	***-24.84***	***3.272***	12.40	***5.824***

Table 6.5: Variation in spec due to faulty Resistor R_c across Capacitor C (10pF)

a small value (which would short the two ends of the resistor). It is seen from Table 6.5 that at around 5K, S11 and Noise Figure (NF) deteriorated beyond the 10% limit affecting circuit's functionality. By reducing the resistance further to a very low value (100Ω) which simulates a short, it is seen that almost all the parameters except for voltage gain have changed beyond the acceptable tolerance limits. This is quite intuitive because of the role the DC blocking capacitor plays in the functionality of the LNA.

The source degenerate transistor is added to match the impedances at the input. A defect falling on the transistor is modeled as a faulty resistor. This resistive effect of the defect changes the effective impedance of the system at resonance and causes degradation in S11 as can be seen in Table 6.6. Any defect falling on the transistor and shorting the Gate-Source changes the transconductance of the transistor B and hence the overall transconductance Gm or the Gain of the Stage which is given by S21.

Tables 6.7 – 6.9 indicate the locations of the bridges which were formed on the inductor using the ASITIC tool and the corresponding inductance values which are obtained.

R_B	S11 dB	S12 Db	S21 dB	V G dB	NF dB
NR	-17.79	-34.31	10.64	13.14	0.824
10 K	***-13.03***	-33.75	***6.939***	13.02	***1.574***
100 Ω	***-0.8175***	-33.19	***-33.1***	***-22.3***	***1.675***

Table 6.6: Variation in spec due to faulty Resistor R_b across Capacitor C (10pF)

Segments Bridged	Faulty Inductance (L_s 1.4nH) value
Segments 1,5,9 & Segments 4,8,12	Ls = 1.374nH
Segments 1,5,9 & Segments 2,6,10	Ls = 1.38nH
Segments 2,6,10 & Segments 3,7,11	Ls = 1.24nH
Segments 3,7,11 & Segments 1,5,9	Ls = 1.25nH
Segments 12 & Segments 3,7,11	Ls = 1.19nH

Table 6.7: Bridge by a defect on L_s

6.2 Cost Model Results

A study was done on a generic chip with data obtained from [33],[10]. Though a few parameters were not available for research, some calculated assumptions which are verified through the obtained results were made. Tables 6.10–6.12 indicate the silicon, personnel and the escape cost for various reliabilities of the system which are varied from 0.1-0.8. The total cost of a chip for manufacturing and also servicing it on site is given as 2100000 dollars. This was decided on a heuristic basis taking into account the manufacturing cost of a variety of chips available in the literature and averaging them out for similar gate count devices. All the costs included in the tables below are in dollars. Hence the net effective price for including fault tolerance on chip is given in Table 6.14. Figures 6.6 and 6.7 are a graphical representation of the data presented in Tables 6.13 and 6.14.

Segment Bridged	Faulty Inductance (L_g 14nH) value
Segments 1,5,9,13,17,21,25 & Segments 4,8,12,16,20,24,28	13.86nH
Segments 1 to 25 & Segments 2,6,10,14,18,22, 26	13.82nH
Segments 2 to 26 & Segments 3 to 27	13.4nH
Segments 3,7	13nH
Segments 3,7,11,15,19,23, 27	13.2nH
Segment 1	13.4nH
Segments 4,8,12,16,20,24,28	13.6nH

Table 6.8: Bridge by a defect on L_g

Segments Bridged	Faulty Inductance (L_d 7nH) value
Segment 1	6.8nH
Segments 1,5,9,13,17,21	7nH
Segments 1,5,9,13,17,21 & Segments 2,6,10,14,18,22	6.2nH
Segments 3,7,11,15,19,23 & Segments 4,8,12,16,20,24	6nH
Segments 3,7,11,15,19,23	6.54nH
Segments 2,6,10,14,18,22	6.88nH
Segments 1,5,9,13,17,21 & Segments 4,8,12,16,20,24 & Segments 2,6,10,14,18,22 & Segments 3,7,11,15,19,23	6.82nH
Segments 1,5,9,13,17,21(at the end) & Segments 2,6,10,14,18,22 & Segments 4,8,12,16,20,24 & Segments 3,7,11,15,19,23 (at the end)	6.66nH

Table 6.9: Bridge by a defect on L_d

Reliability	0.15	0.25	0.45	0.65	0.75	0.8
Silicon Cost	621000	667000	759000	851000	917700	920000

Table 6.10: Silicon Cost for the Generic chip

Reliability	0.15	0.25	0.45	0.65	0.75	0.8
Escape Cost	256000	236000	196000	156000	136000	126000

Table 6.11: Escape Cost for the Generic chip

In Fig. 6.5, one can see that as reliability increases, so does the silicon cost. This is attributed to the increase in area of the chip due to the added logic. Also, there is a drop in escape costs due to a higher degree of reliability. The third cost is the personnel cost. Though this cost does increase due to increase in design time, it is fairly compensated by the limited amount of work required to be done in the form of service/repair. Hence, there seems to be a dip in the graph due to increased benefits of fault tolerance and hence an increase in the savings.

In Fig. 6.6, a net calculation of the cost with fault tolerance and without it has been done. The tester cost for both the systems (with and without fault tolerance and DFT) is fixed up to be the same since the time saved in testing through the inclusion of DFT is increased by the added logic which appears in the form of redundant logic. It is seen that with higher reliability the unit with fault tolerance has a far greater cost advantage than the unit without fault tolerance while with lower reliability the reverse trend can be observed.

The conclusion from the above plot is that for this particular chip, it is better to go for a high reliability system in order to save on after sales services and also ensure good customer relationship.

Reliability	0.15	0.25	0.45	0.65	0.75	0.8
Personnel Cost	716000	680000	512000	376000	320000	312000

Table 6.12: Personnel Cost for the Generic chip

Reliability	0.15	0.25	0.45	0.65	0.75	0.8
Total Cost	2293000	2283000	2167000	2083000	2073700	2058000

Table 6.13: Total Cost for the Generic chip

In the study involving the RF core, the realestate for a wide range of reliability values was first established. In Table 6.15, one can see the trend of increasing silicon costs due to an increase in the area of the chip. The escape cost drop in Table 6.16 is also on expected lines since the reliability has increased. But there is a slight dip in the personnel costs in Table 6.17 due to the lower interaction of the service personnel with the chip on-site. This is because of the optimum reliability offered by the chip that the chance of it failing is minimized and the area overhead is also bearable. At high reliability the cost of the silicon is too high to be compensated by fault tolerance. One could thus strike a good balance between the cost of silicon as well as reliability and the other cost involved by studying the data in advance, before going on to make any critical decisions with respect to the chip design.

The total cost of a chip for manufacturing and also servicing it on site is given as 1300000 dollars. Again heuristics was used as mentioned in the previous section to finalize the total manufacturing cost. The nett effective price for including fault tolerance on chip is given in Table 6.19. Fig. 6.8 is a reflection of what has been said above. It shows that with a reliability of around 0.5-0.6 one is guaranteed of a cost effective chip. Thus the cost model would help in modeling design issues by factoring the reliability of the chip into the cost model.

Reliability	0.15	0.25	0.45	0.65	0.75	0.8
Net Excess Cost	193000	183000	67000	-17000	-26300	-42000

Table 6.14: Net Excess Cost for the Generic chip

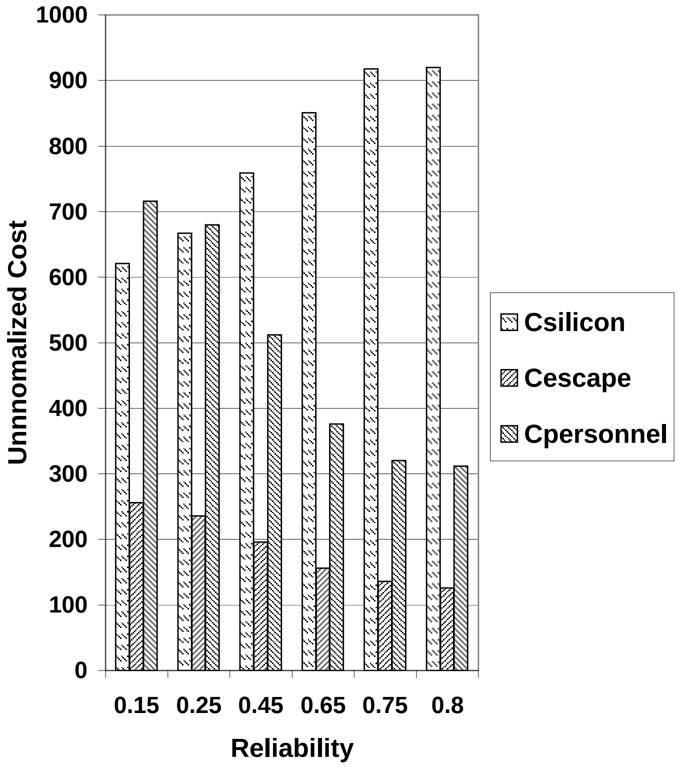

Figure 6.5: Cost vs Reliability - Generic Chip

Reliability	0.2	0.3	0.4	0.5	0.6	0.7	0.8
Silicon Cost	552000	598000	644000	690000	736000	782000	828000

Table 6.15: Silicon Cost for the SOC chip

Reliability	0.2	0.3	0.4	0.5	0.6	0.7	0.8
Escape Cost	246000	226000	206000	156000	150000	146000	126000

Table 6.16: Escape Cost for the SOC chip

Reliability	0.2	0.3	0.4	0.5	0.6	0.7	0.8
Personnel Cost	650400	572160	538432	360000	391568	587840	489600

Table 6.17: Personnel Cost for the SOC chip

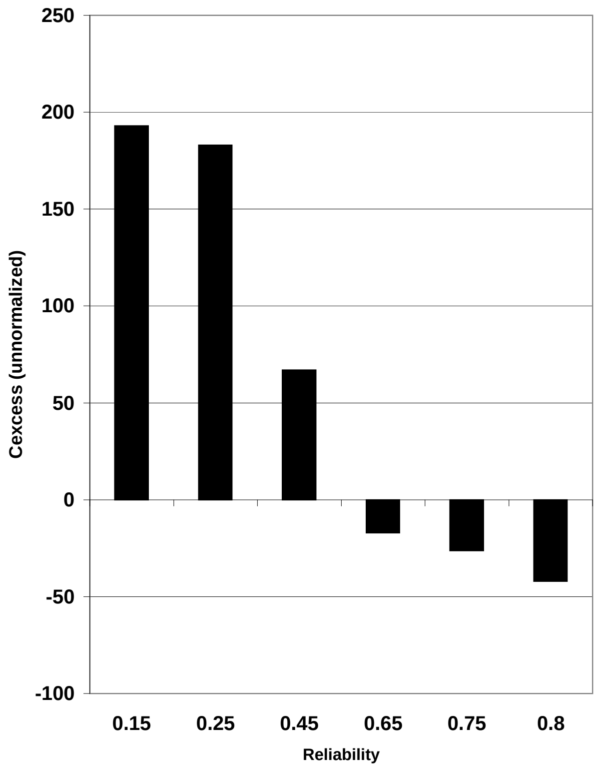

Figure 6.6: Excess Cost vs Reliability - Generic Chip

Reliability	0.2	0.3	0.4	0.5	0.6	0.7	0.8
Total Cost	1448400	1396160	1388432	1206000	1277568	1515840	1443600

Table 6.18: Total Cost for the SOC chip

Reliability	0.2	0.3	0.4	0.5	0.6	0.7	0.8
Nett Excess Cost	148400	96160	88432	-94000	-22432	215840	143600

Table 6.19: Nett Excess Cost for the SOC chip

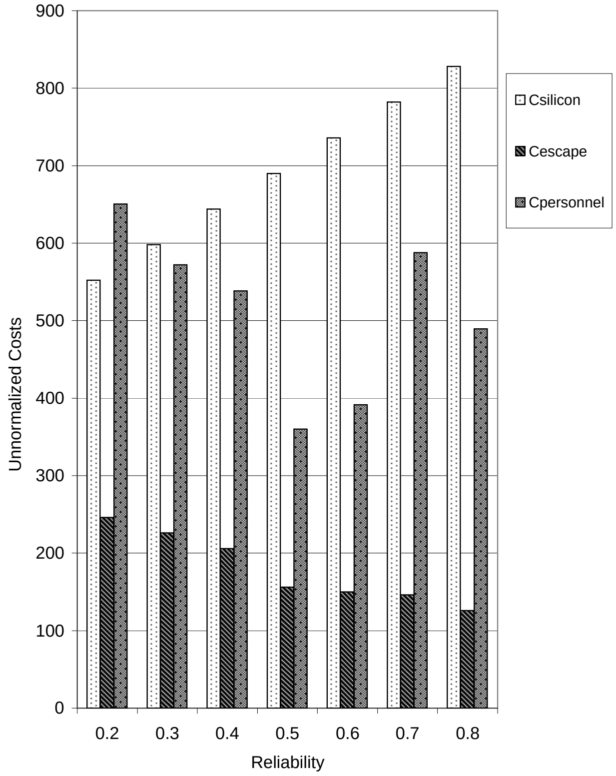

Figure 6.7: Cost vs Reliability - Mixed IP core

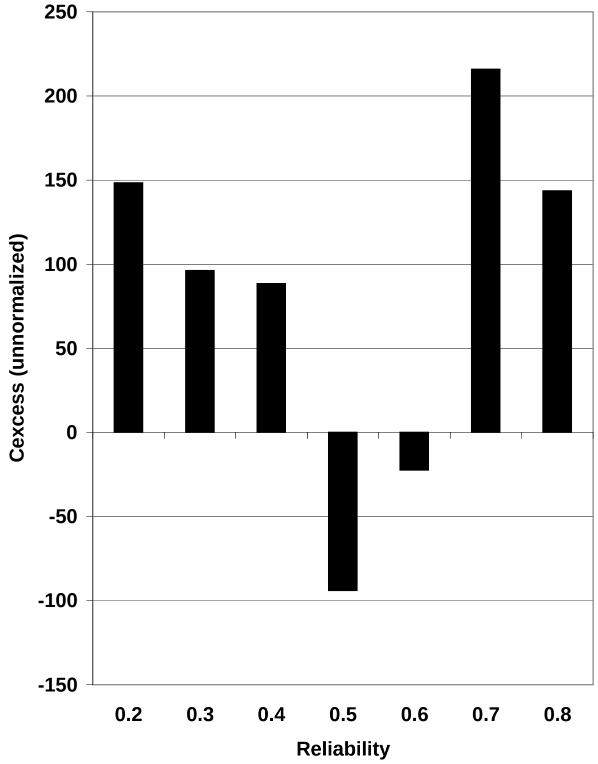

Figure 6.8: Excess Cost vs Reliability - Mixed IP core

Chapter 7

Conclusion

7.1 Summary of Contributions

With the growing problem of RLC's arising from interconnects as parasitics, one has to take careful design measures while building high frequency devices. When we design resistors, inductors and capacitors, due to the high frequency of operation, the 10% tolerance limit is not necessarily good enough to ensure a fault-free circuit [43]. Hence some leeway must be given while designing such components to take the parasitics into account.

A new fault model is proposed for inductors and the resistive fault models proposed in [23] are verified in the context of RF circuits. Defect based fault modeling is justified to give good fault models for RF circuits. To date there is no detailed defect analysis for RF circuits as described in this thesis. Due to the large size of these devices the chances of a defect falling on these passive components is the highest. Also the designer needs to go for more stringent tolerance limits for the circuit parameters while going for high speed and ultra

DSM technology.

With regards to the economic side to DFM, a cost model for a fault tolerant chip taking DFT into account, is proposed. The model provides flexibility to handle different types of costs that may arise during the life cycle of a chip. It focuses on tying together issues on design, test and time to market in order to decide on a chip's feature. Bringing the reliability factor into the model ensures that we are able to study the cost of the chip throughout its life cycle. Its flexibility can be seen from the fact that we can model not only fault tolerant chips, but also DFT based systems by excluding the required factors in overall cost equation. The model is intended to aid project team managers to make certain decisions on a chip before initiating work.

7.2 Future Work

As a future work one can look at how defects combined in multiple components affect the working of the circuit as most of these components are ratioed. Any defect in one of the components could be compensated by a defect in another component or could further degrade the performance. Breaks are not yet fully understood and is an issue which can be handled as a future work.

From an economic perspective related to DFM the psychological effects on cost equations, effects of outsourcing and productivity issues related to designers are some areas which require more study and is suggested as a future work.

Appendix A

A.1 Fault Set from CARAFE

The following files have already been described in detail in the previous chapters and an in-depth coverage is available in the Carafe manual [17]. For the readers convenience the sim files have been converted to spice using the sim2spice tool available in the Magic package. The defect statistics file is given below.

```
fab
scmos
end

types
polysilicon
ntransistor
ptransistor
active
metal1
metal2
```

```
diffcut
pc
m2c
pad
end

gos
ntransistor 1.0
ptransistor 1.0
end

radius
250
end

bridge
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
```

```
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
end

break
1.0
1.0
1.0
1.0
1.0
1.0
1.0
1.0
1.0
1.0
end

radius
450
end

bridge
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
```

```
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
end

break
1.0
1.0
1.0
1.0
1.0
1.0
1.0
1.0
1.0
1.0
end

radius
```

```
950
end

bridge
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0
end

break
1.0
1.0
1.0
1.0
1.0
1.0
1.0
```

```
1.0
1.0
1.0
end
```

The spice file of the fault-free LNA.

```
* Extracted spice deck
* for su-bicmos you should get the .sim file using ext2simBiCMOS
* Units: 0.010000, Technology: scmos
* Units: 0.010000, Technology: Carafe
* Units: 0.010000, Technology: Mon
M1 M3_0/s3 M3_0/g3 M2_0/s2 Gnd  NMOS W=500.1U L=0.6U
+ AD=0P PD=0U AS=0P PS=0U
M2 M2_0/s2 vddX d2 Gnd  NMOS W=500.1U L=0.6U
+ AD=0P PD=0U AS=0P PS=0U
M3 gndX vddX vddX Gnd  NMOS W=50.1U L=0.6U
+ AD=0P PD=0U AS=0P PS=0U
```

The spice file containing the details of the location of the bridges in the circuit.

```
* Extracted spice deck
* for su-bicmos you should get the .sim file using ext2simBiCMOS
* Units: 0.010000, Technology: scmos
* Units: 0.010000, Technology: Carafe
* Units: 0.010000, Technology: defect
* Units: 0.010000, Technology: Mon
M1 M3_0/s3 M3_0/g3 M2_0/s2 Gnd  NMOS W=500.1U L=0.6U
+ AD=0P PD=0U AS=0P PS=0U
M2 M2_0/s2 vddX d2 Gnd  NMOS W=500.1U L=0.6U
+ AD=0P PD=0U AS=0P PS=0U
M3 gndX vddX vddX Gnd  NMOS W=50.1U L=0.6U
+ AD=0P PD=0U AS=0P PS=0U
Q1 M3_0/g3 gndX brg_0 b4x2 1000
Q2 gndX vddX brg_0 b4x2 1000
Q3 c1 vddX brg_1 b4x2 1000
Q4 M3_0/g3 gndX brg_2 b4x2 1000
Q5 M3_0/s3 gndX brg_3 b4x2 1000
Q6 M3_0/g3 vddX brg_4 b4x2 1000
Q7 gndX vddX brg_5 b4x2 1000
Q8 d2 gndX brg_6 b4x2 1000
Q9 d2 vddX brg_7 b4x2 1000
Q10 M3_0/g3 d2 brg_8 b4x2 1000
Q11 d2 vddX brg_8 b4x2 1000
```

The fault list containing the probability of occurrence of each fault.

```
# m4_f.pro generated by Carafe Version Alpha.5
# faults extracted with defect radii of: 950, 450, 250 centimicrons.
fault: brg_1 brg: (c1 vddX)
             rank: 1 prob: 0.799994 total: 5768151552.000
             layer: polysilicon to metal1       1.000  5768151552.000
fault: brg_4 brg: (M3_0/g3 vddX)
             rank: 2 prob: 0.078418 total: 565412992.000
             layer: metal1      to metal2       0.865  489110592.000
             layer: polysilicon to polysilicon  0.014  7663900.000
             layer: metal1      to metal1       0.031  17429900.000
             layer: metal2      to metal2       0.091  51208700.000
fault: brg_7 brg: (d2 vddX)
             rank: 3 prob: 0.047504 total: 342512736.000
             layer: metal1      to metal2       0.965  330649952.000
             layer: metal1      to metal1       0.035  11862800.000
fault: brg_3 brg: (M3_0/s3 gndX)
             rank: 4 prob: 0.023532 total: 169674080.000
             layer: metal1      to metal2       0.984  166932000.000
             layer: metal1      to metal1       0.016  2742100.000
fault: bb_2 brk: (M3_0/g3_0 M3_0/g3_1)
            brk: (vddX_3 vddX_7)
            brg: (M2_0/s2_0 M3_0/s3_0 d2_0)
            rank: 5 prob: 0.011905 total: 85840608.000
```

```
            layer: ntransistor  1.000  85840608.000
fault: bb_0 brk: (M3_0/g3_0 M3_0/g3_1)
            brg: (M2_0/s2_0 M3_0/s3_0)
            rank: 6 prob: 0.010355 total: 74662600.000
            layer: ntransistor  1.000  74662600.000
fault: bb_1 brk: (vddX_3 vddX_7)
            brg: (M2_0/s2_0 d2_0)
            rank: 7 prob: 0.010355 total: 74662600.000
            layer: ntransistor  1.000  74662600.000
fault: brk_11 brk: (vddX_5 vddX_6)
              rank: 8 prob: 0.007372 total: 53155072.000
              layer: polysilicon  0.178  9438000.000
              layer: pc           0.207  10995600.000
              layer: metal2       0.230  12246950.000
              layer: metal1       0.227  12051050.000
              layer: m2c          0.158  8423475.000
fault: bb_3 brk: (vddX_0 vddX_4)
            brg: (gndX_0 vddX_1)
            rank: 9 prob: 0.002788 total: 20103200.000
            layer: ntransistor  1.000  20103200.000
fault: brg_5 brg: (gndX vddX)
             rank: 10 prob: 0.002778 total: 20027700.000
             layer: metal1      to metal2       0.269  5395400.000
             layer: metal1      to metal1       0.731  14632300.000
```

```
fault: brg_8 brg: (M3_0/g3 d2 vddX)
             rank: 11 prob: 0.001314 total: 9476600.000
             layer: metal1      to metal2       1.000  9476600.000
fault: brk_2 brk: (vddX_4 vddX_5)
             rank: 12 prob: 0.001239 total: 8936600.000
             layer: polysilicon  0.341  3049900.000
             layer: pc           0.404  3612400.000
             layer: metal1       0.254  2274300.000
fault: brk_1 brk: (vddX_4 vddX_5)
             brk: (vddX_5 vddX_6)
             rank: 13 prob: 0.000761 total: 5484600.000
             layer: polysilicon  0.344  1884700.000
             layer: pc           0.123  672400.000
             layer: metal1       0.534  2927500.000
fault: brk_10 brk: (vddX_1 vddX_5)
              rank: 14 prob: 0.000598 total: 4311800.000
              layer: metal1       0.006  27000.000
              layer: diffcut      0.994  4284800.000
fault: brk_6 brk: (vddX_2 vddX_6)
             brk: (vddX_6 vddX_7)
             rank: 15 prob: 0.000591 total: 4258000.000
             layer: polysilicon  1.000  4258000.000
fault: brk_4 brk: (vddX_1 vddX_5)
             brk: (vddX_4 vddX_5)
```

```
              brk: (vddX_5 vddX_6)
              rank: 16 prob: 0.000171 total: 1232500.000
              layer: metal1       1.000  1232500.000
fault: brg_6 brg: (d2 gndX)
              rank: 17 prob: 0.000162 total: 1171600.000
              layer: metal1      to metal1       1.000  1171600.000
fault: brk_0 brk: (vddX_6 vddX_7)
              rank: 18 prob: 0.000053 total: 379800.000
              layer: polysilicon  1.000  379800.000
fault: brk_9 brk: (vddX_2 vddX_6)
              rank: 19 prob: 0.000050 total: 360600.000
              layer: polysilicon  1.000  360600.000
fault: brg_0 brg: (M3_0/g3 gndX vddX)
              rank: 20 prob: 0.000046 total: 331700.000
              layer: metal1      to metal1       1.000  331700.000
fault: brk_8 brk: (vddX_1 vddX_5)
              brk: (vddX_5 vddX_6)
              rank: 21 prob: 0.000006 total: 40500.000
              layer: metal1       1.000  40500.000
fault: brk_5 brk: (vddX_2 vddX_6)
              brk: (vddX_5 vddX_6)
              rank: 22 prob: 0.000003 total: 19200.000
              layer: polysilicon  1.000  19200.000
fault: brk_3 brk: (vddX_2 vddX_6)
```

```
              brk: (vddX_5 vddX_6)
              brk: (vddX_6 vddX_7)
              rank: 23 prob: 0.000002 total: 16000.000
              layer: polysilicon  1.000  16000.000
fault: brk_7 brk: (vddX_1 vddX_5)
              brk: (vddX_4 vddX_5)
              rank: 24 prob: 0.000002 total: 13200.000
              layer: metal1       1.000  13200.000
fault: brg_2 brg: (M3_0/g3 gndX)
              rank: 25 prob: 0.000002 total: 11700.000
              layer: metal1      to metal1       1.000  11700.000
# End of fault list
```

A.2 ASITIC Commands

The commands used in ASITIC are listed below. The number of turns required for the inductor, turn spacing and width and the outer diameter of the coil were calculated using the spiral calculator which is available at http://smirc.stanford.edu/spiralcalc.html. To draw an inductor Ls the following command was used

```
SQ NAME=a:LEN=130:W=7:S=5:N=3:METAL=M3:EXIT=M1:XORG=200:YORG=200
```

For generating bridges, wires of size 65x65 was used. The command used to create the wires.

```
WIRE NAME=C:LEN=65:WID=65:METAL=M3:XORG=223:YORG=300
```

The command used to see how the inductance would change due to a metal1 type defect falling on the wire is given below.

```
WIRE NAME=C:LEN=65:WID=65:METAL=M1:XORG=220:YORG=300
```

The Lg (14nH) was created as a spiral inductor using the following command.

```
SQ NAME=a:LEN=256:W=6:S=4:N=7:METAL=M3:EXIT=M1:XORG=200:YORG=200
```

The following command is used to induce bridges in the inductor.

```
WIRE NAME=C:LEN=65:WID=65:METAL=M3:XORG=223:YORG=300
```

Command to create the Ld inductor is

```
SQ NAME=a:LEN=196:W=6:S=4:N=6:METAL=M3:EXIT=M1:XORG=200:YORG=200
```

The command to create bridges in a required area is

```
WIRE NAME=C:LEN=65:WID=65:METAL=M3:XORG=223:YORG=300
```

The command to find out the inductance value at a particular frequency is

```
indmat a 1.5G
```

Segment 1 is the segment which gets the current first, then the subsequent segments are numbered in the order it recieves current. The last segment would be the one through which the current leaves the inductor. The above bridges which are inserted in the inductor are shown in Figures 3.2, 3.3, 6.2, 6.3 and 6.4.

Bibliography

[1] J. Liu, "Detailed Model Shows FPGA's True Costs," *EDN*, pp. 153–158, May 11, 1995.

[2] M. Levitt, "Economic and Productivity Considerations in ASIC Test and Design for Test," in *Proceedings of Compcon*, pp. 440–445, 1992.

[3] W. Maly, H. Heineken, J. Khare, and P. Nag, "Design for Manufacturability in Submicron Domain," in *Computer-Aided Design, Digest of Technical Papers., 1996 IEEE/ACM International Conference on*, pp. 690 – 697, 10-14 Nov. 1996.

[4] "Design for Manufacturability [ITC 2003 Roundtable]," in *Design and Test of Computers, IEEE*, vol. 21, pp. 144 – 156, March-April 2004.

[5] J. Shen, W. Maly, and F. Ferguson, "Inductive Fault Analysis of MOS Integrated Circuits," in *IEEE Design and Test*, pp. 33–26, Dec. 1985.

[6] "Semiconductor Industry Association International Technology Roadmap for Semiconductors," *Test and Test Equipment*, 2003.

[7] K. P. White and W. Trybula, “Design for Semiconductor Manufacturing – Perspective,” in *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, vol. 20, pp. 58–72, Jan. 1997.

[8] R. Wilcox, T.Forhan, G.Starkey, and D.Turner, “Design for Manufacturability – A Key to Semiconductor Excellence,” in *IEEE/SEMI Advanced Semiconductor Manufacturing Conference*, pp. 308–313, Sept. 1998.

[9] L.Y.Ungar and T. Ambler, “Economics of Built In Self Test,” in *Design and Test of Computers*, vol. 18, pp. 70–79, Sept-Oct. 2001.

[10] P. Nag, A. Gattiker, S. Wei, R. Blanton, and W. Maly, “Modeling the Economics of Testing: a DFT Perspective,” in *Design and Test of Computers, IEEE*, pp. 29–41, Jan-Feb. 2002.

[11] N. Mokhoff, “Life Long Testing Prescribed for Chips,” *EETimes*, Oct. 2003.

[12] M. Bushnell and V. Agrawal, *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*. Kluwer Academic Publishers, 1 ed., 2000.

[13] A. V. de Goor, *Testing Semiconductor Memories : Theory and Practice*. J. Wiley and Sons, 1 ed., 1995.

[14] P. Nagaraj, S. Upadhyaya, K. Zarrineh, and D. Adams, “Defect Analysis and a New Fault Model for Multi-Port SRAMs,” in *Defect and Fault Tolerance in VLSI Systems, Proceedings. 2001 IEEE International Symposium on*, pp. 366 – 374, 24 – 26 Oct 2001.

[15] J. Khare and W. Maly, *From Contamination to Defects, Faults and Yield loss, Simulation and Applications*. Kluwer Academic Publishers, 1 ed., 1996.

[16] A. Jee and F. Ferguson, “Carafe: An Inductive Fault Analysis Tool for CMOS VLSI Circuits,” in *VLSI Test Symposium*, pp. 92 –98, 6-8 April 1993.

[17] A. Jee, D. Dahle, C. Bazeghi, and F. Ferguson, “Carafe User’s Manual,” 1996.

[18] T. Mak, “Private Communication,” Oct. 2003.

[19] F. Ferguson, “Private Communication,” Oct. 2003.

[20] M. Soma, “An Experimental Approach to Analog Fault Models,” in *IEEE Int. Conf. Custom Integrat. Circuits*, 1991.

[21] M. Soma, “Fault Models for Analog-to-Digital Converters,” in *IEEE Pacific Rim Conference on Communications, Computers and Signal*, vol. 2, pp. 503 –505, 9-10 May 1991.

[22] H.-C. Liu and M. Soma, “Fault Diagnosis for Analog Integrated Circuits Based on the Circuit Layout,” in *Fault Tolerant Systems, Proceedings, Pacific Rim International Symposium*, pp. 134 – 139, Sept. 1991.

[23] M. Soma, “Fault Modeling and Testing Generation for Sample-and-Hold Circuits,” in *Circuits and Systems, IEEE International Symposium on*, vol. 4, pp. 2072 – 2075, 11-14 June 1991.

[24] M. Sachdev and B. Atzema, “Industrial Relevance of Analog IFA: Fact or Fiction,” in *Proceedings of the International Test Conference*, 1995.

[25] T. Mak, D. Bhattacharya, C. Prunty, B. Roeder, N. Ramadan, J. Ferguson, and J. Yu;, “Cache RAM Inductive Fault Analysis with Fab Defect Modeling,” in *International Test Conference*, pp. 862 –871, 18-23 Oct. 1998.

[26] C.Metra, S. D. Francescantonio, and T. Mak, "Clock Faults Impact on Manufacturing Testing and Their Possible Detection Through On-line Testing," in *Test Conference, Proceedings International*, pp. 100 – 109, 7-10 Oct. 2002.

[27] S. Zachariah and S. Chakravarty, "A Novel Algorithm for Multi-Node Bridge Analysis of Large VLSI Circuits," in *VLSI Design Fourteenth International Conference on*, pp. 333 – 338, 3-7 Jan. 2001.

[28] A. Niknejad, "Modeling of Passive Elements with ASITIC," in *Radio Frequency Integrated Circuits Symposium*, pp. 303 – 306, 2-4 June 2002.

[29] *Cadence SpectreRF User Guide - Cadence Design Suite.*

[30] A. Niknejad and R. Meyer, "Analysis, Design, and Optimization of Spiral Inductors and Transformers for Si RF ICs," in *Solid-State Circuits, IEEE Journal of*, vol. 33, pp. 1470 – 1481, Oct. 1998.

[31] K. Sundararaman, S. Upadhyaya, and S. Narayanan, "Defect Analysis and Fault Model Extensions for RF Circuits," in *13th North Atlantic Test Workshop*, 13–14 May 2004.

[32] J.-M. Lu and C.-W. Wu, "Cost and Benefit Models for Logic and Memory BIST," in *Design, Automation and Test in Europe Conference and Exhibition 2000. Proceedings*, pp. 710–714, March, 2000.

[33] J. Debardelaben, V. Madisetti, and A. Gadient, "Incorporating Cost Modeling in Embedded-System Design," in *Design and Test of Computers, IEEE*, vol. 14, pp. 24–35, July-Sept. 1997.

[34] N. Hatch and J. Macher, "Mitigating the Time to Market and Performance Tradeoff: Knowledge Management in New Technologies," 2003.

[35] D. Williams and A. Ambler, "System Manufacturing Test Cost Model," *Test Conference, 2002. Proceedings*, pp. 482–490, Oct. 2002.

[36] K. Sundararaman, S. Upadhyaya, and M. Margala, "Cost Model Analysis of DFT Based Fault Tolerant SOC Designs," in *Intl Symposium on Quality Electronic Design*, pp. 465 – 469, 22 – 24 March 2004.

[37] P. Lala, *Self Checking and Fault Tolerant Digital Design*. Morgan Kaufmann, 1 ed., 2001.

[38] Y. Gagnonm, Y. Savaria, M. Meunier, and C. Thibeault, "Are Defect Tolerant Circuits with Redundancy Really Cost-Effective? Complete and Realistic cost model," in *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, pp. 157–165, Oct. 1997.

[39] T. Michalka, W. Lukaszek, and J. Meindl, "A Discussion of Yield Modeling with Defect Clustering, Circuit Repair, and Circuit Redundancy," in *Semiconductor Manufacturing, IEEE Transactions on*, vol. 3, pp. 158–167, 1990.

[40] T. Williams and N. Brown, "Defect Level as a Function of Fault Coverage," in *IEEE Trans. Computers*, vol. 30, pp. 987–988, 1981.

[41] R. Mathis, *Corporate Finance Live*. Prentice-Hall, 1 ed., 2000.

[42] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge University Press, 1 ed., 1998.

[43] K. Gala, D. Blaauw, J. Wang, V. Zolotov, and M. Zhao, "Inductance : Analysis and Design Issues," in *38th Design Automation Conference*, pp. 329–334, 18-22 June 2001.